



New Trends in Computational Lithography – Data, Algorithms, and Applications

Yu Cao

ASML-Brion

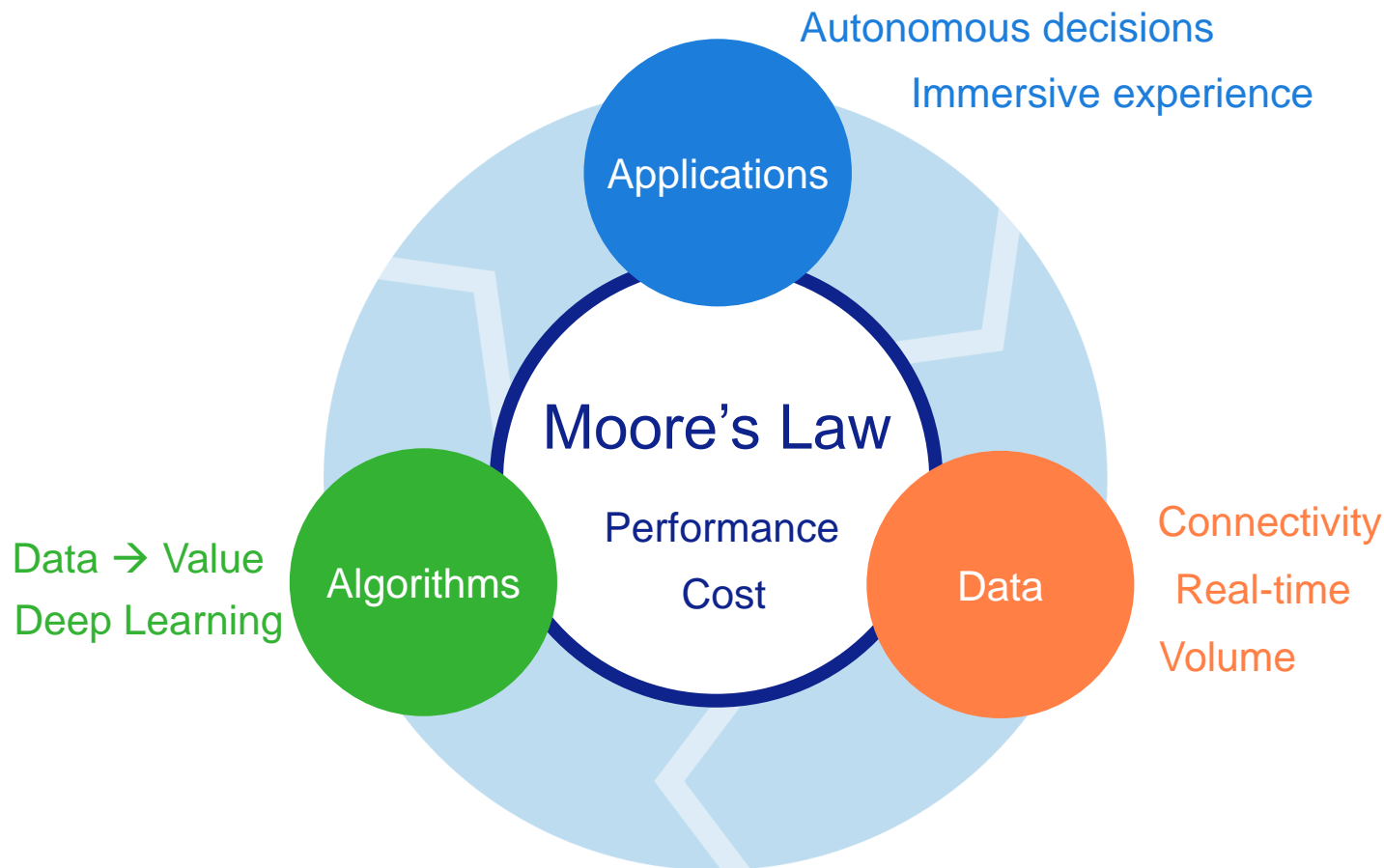
Xiamen, October 2018

- New challenges arise in **accuracy** and **speed** to meet demands in 7nm and beyond
 - Accuracy requirements are approaching single nanometer
 - Worldwide computing power for OPC has exceeded 10 PFLOPS, on par with the world's most powerful supercomputers and incurring substantial cost
- New opportunities enabled by new technologies:
 - New **data** acquisition by fast e-beam metrology systems
 - New **algorithms** for modeling and optimization further empowered by machine learning and new computing architecture
 - New **applications** in patterning equipments including EUV scanners and multi-beam mask writers

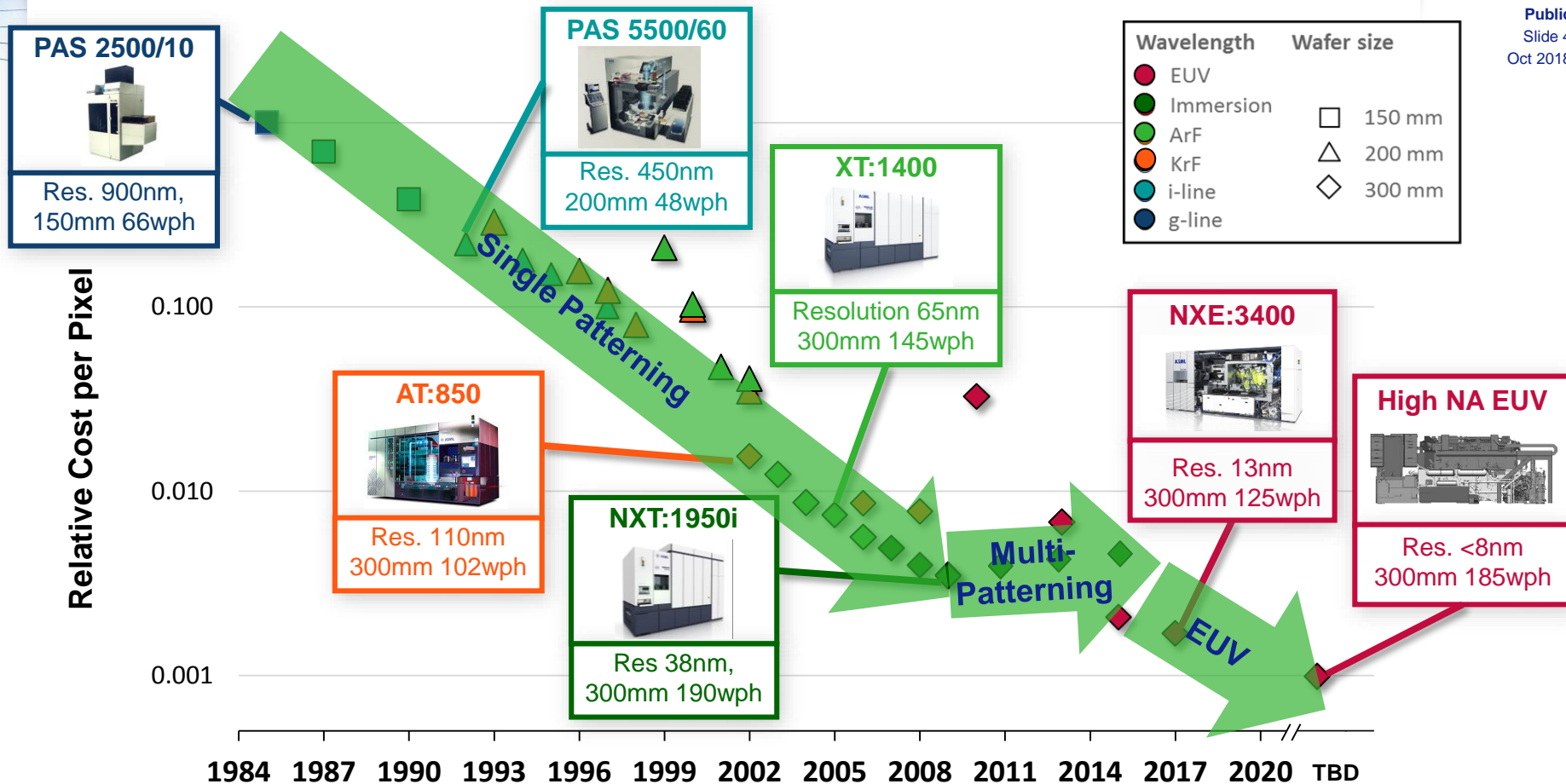
Major trends in semiconductor-enabled computing

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Litho cost reduction continues to drive Moore's Law



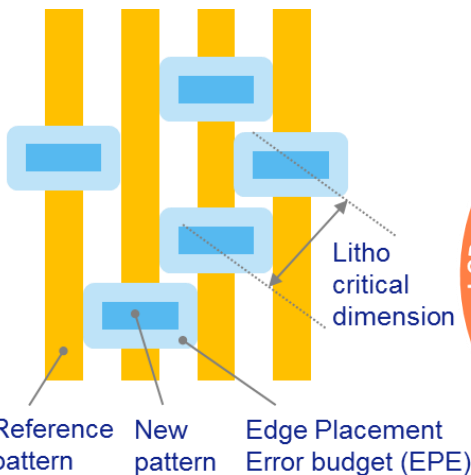
Scaling requires Edge Placement Accuracy improvements

ASML has expanded its focus to address the total litho error

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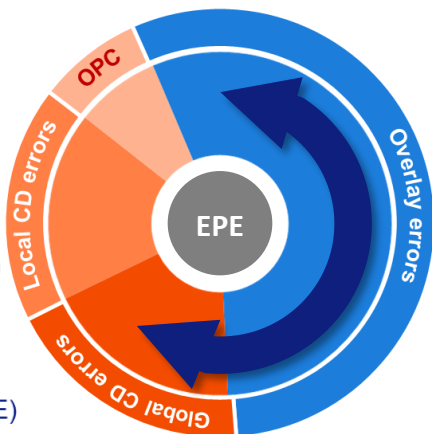
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Device Pattern



2005 65nm Node

XT:1400, ArF, NA 0.93
Single Expose, k_1 0.43

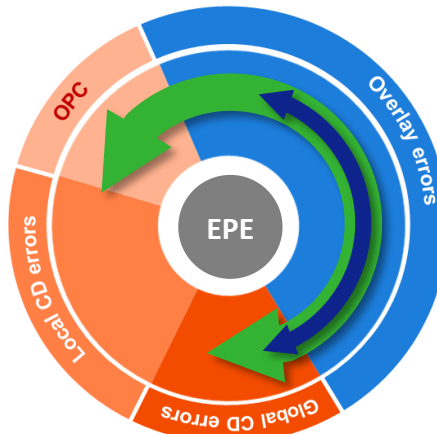


Scanner

>50% of EPE budget

2011 28nm Node

NXT:1950i, ArFi, NA 1.35
Single Expose k_1 0.28



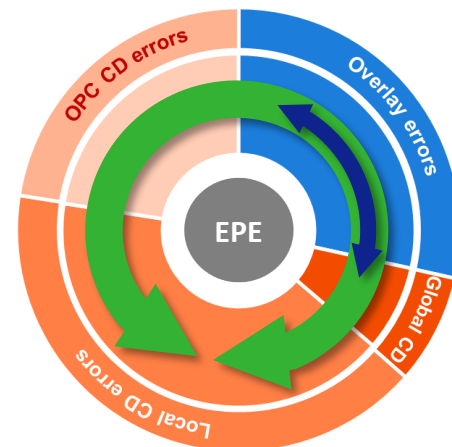
Holistic Lithography

- Brion Computational Litho & OPC
- YieldStar Optical Metrology
- Scanner Feedback and Control

>75% of EPE budget

2019 5nm Node

NXT:2000i-NXE:3400 ArFi-EUV
Multiple Patterning k_1 0.1 - 0.5



Pattern Fidelity Control

- HMI e-beam metrology & inspection
- YieldStar extension post etch, in-die
- Litho-Etch co-optimisation

>90% of EPE budget

ASML contribution

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Holistic Lithography delivering significant customer value

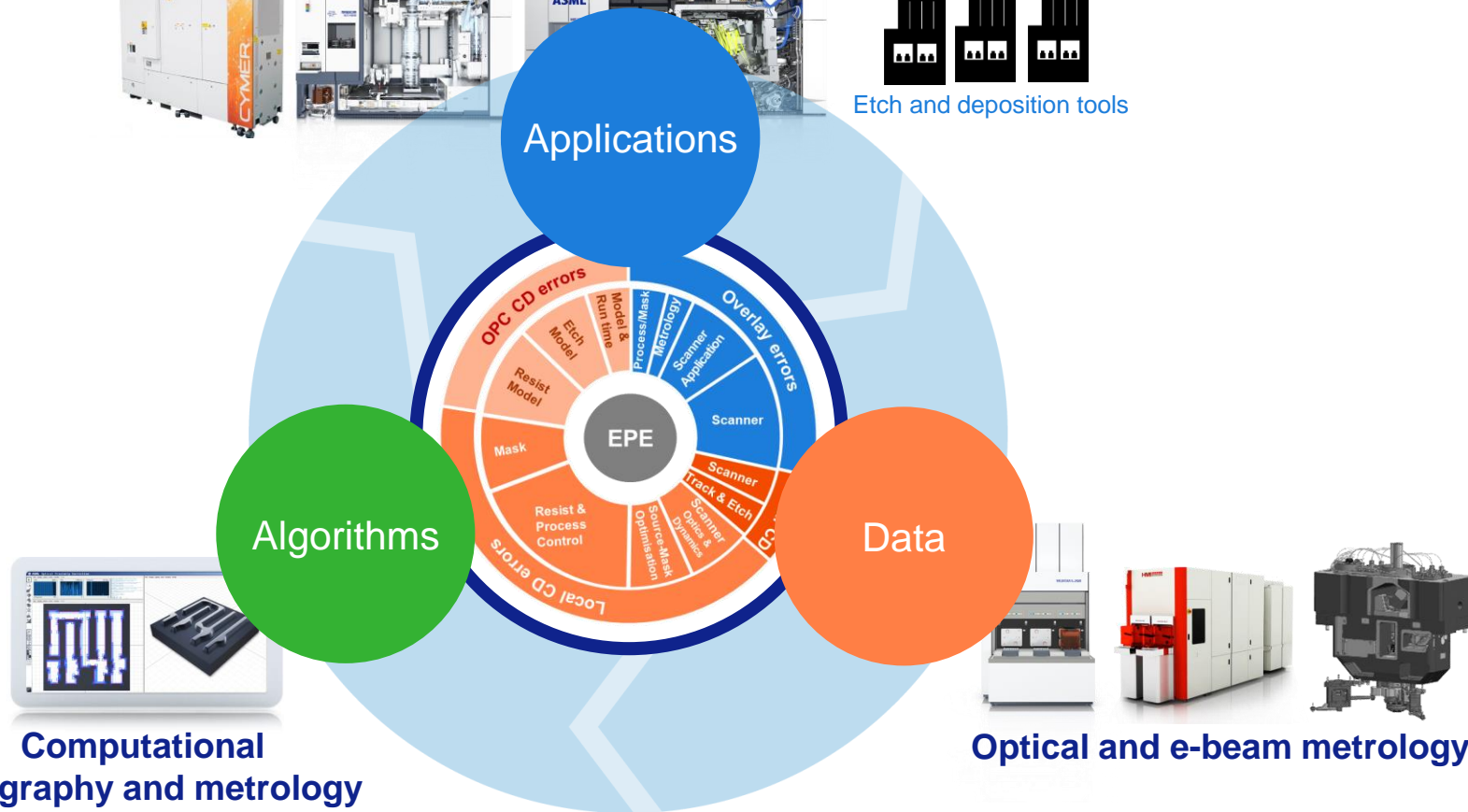
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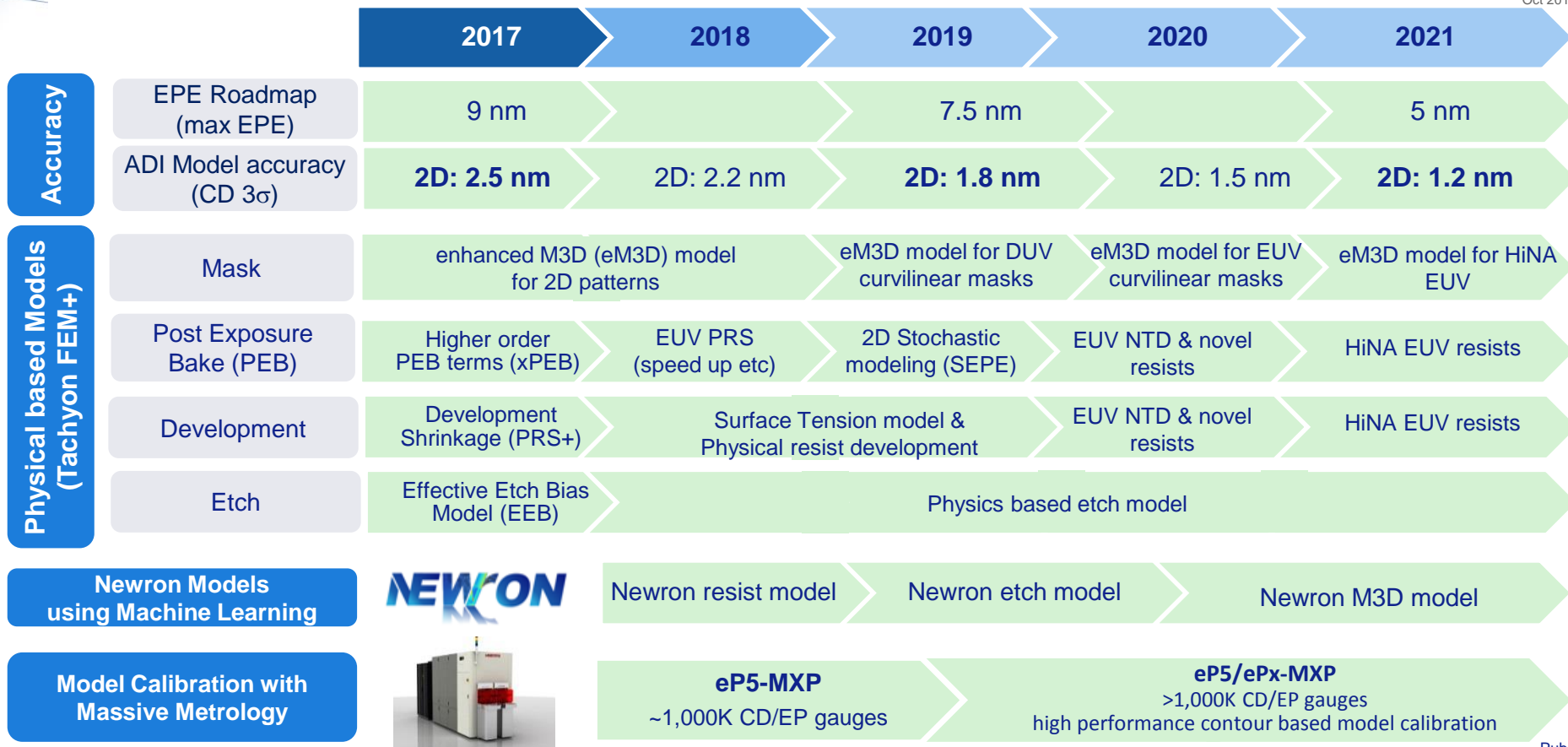
Lithography scanner with advanced control capability



Etch and deposition tools



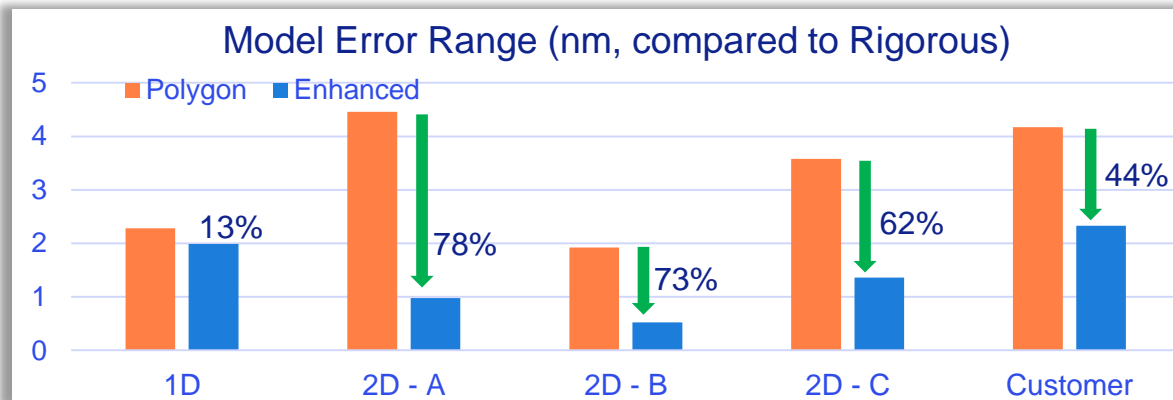
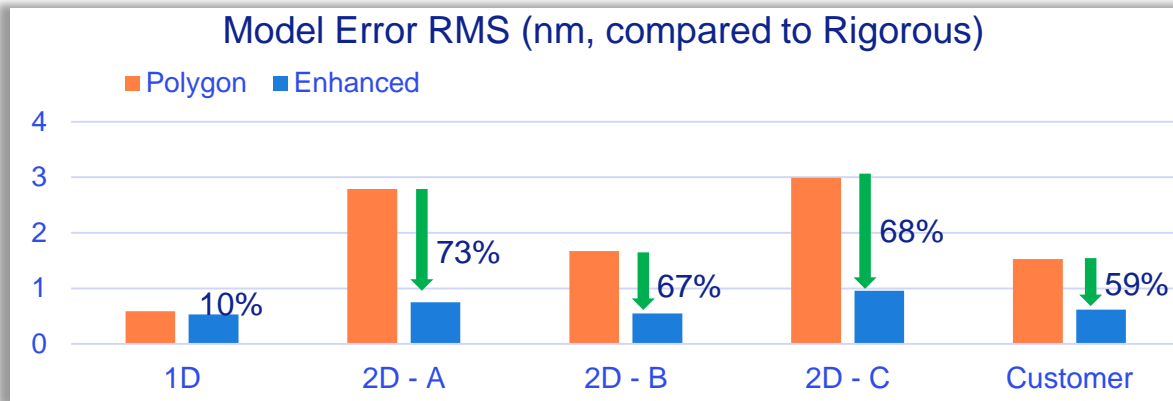
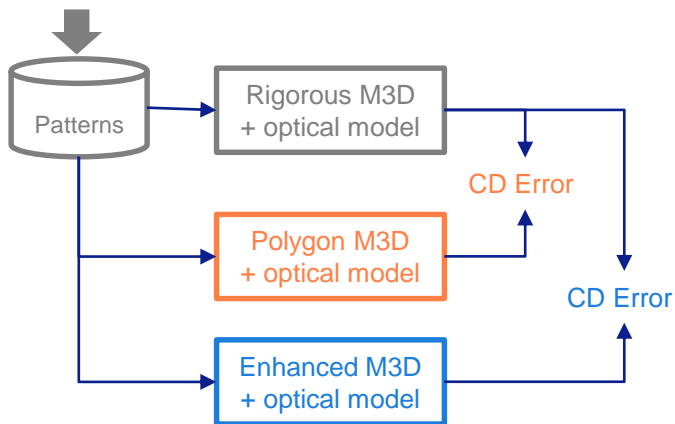
Tachyon model products extend model accuracy roadmap toward single nanometer



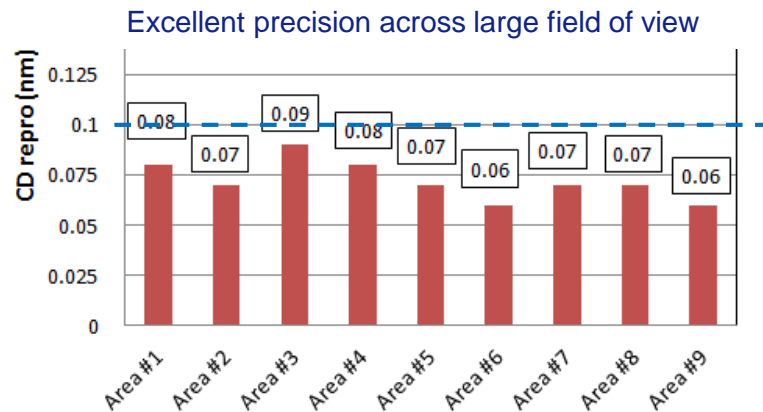
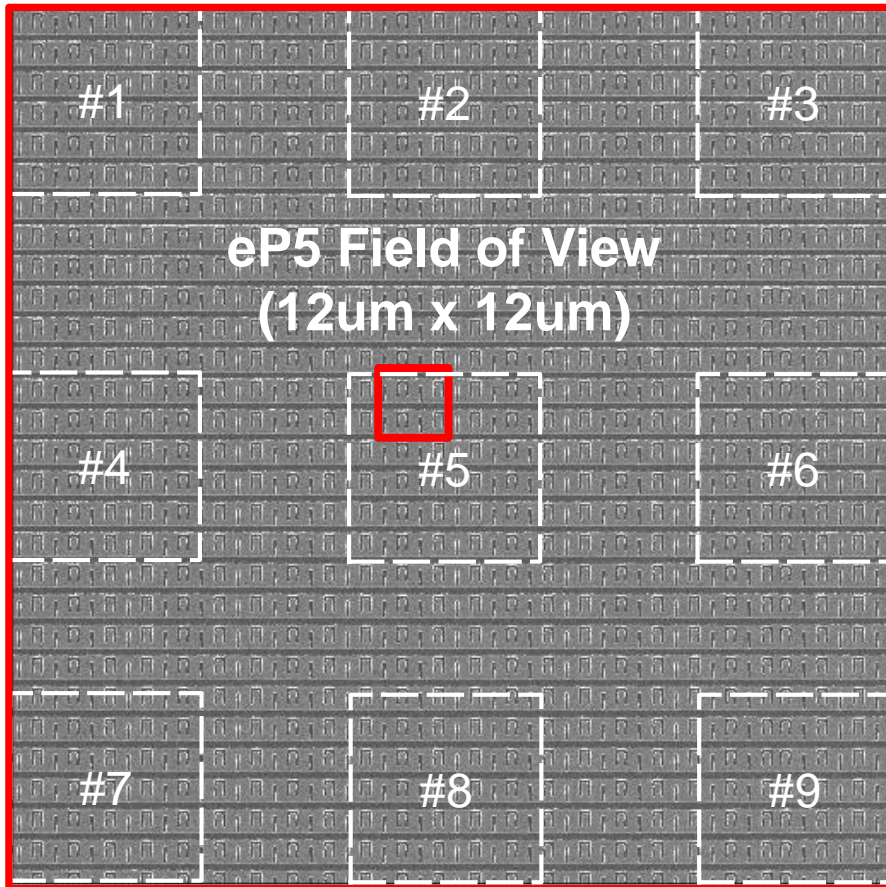
Enhanced 3D mask model delivers significant accuracy benefits

Selected DUV patterns:

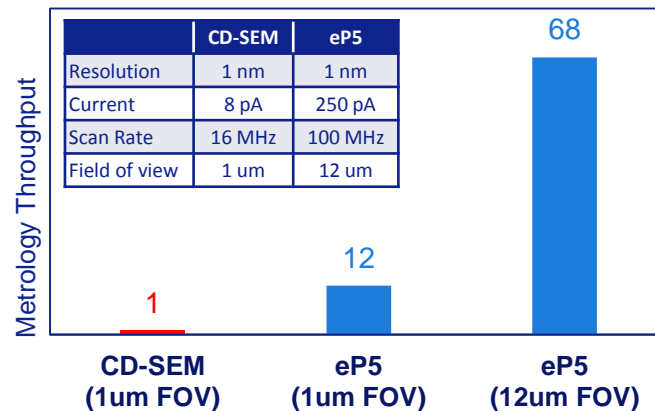
- 1D (82 gauges)
- 2D – A (15 gauges)
- 2D – B (9 gauges)
- 2D – C (9 gauges)
- Customer (48 gauges)



High speed e-beam metrology and large field of view

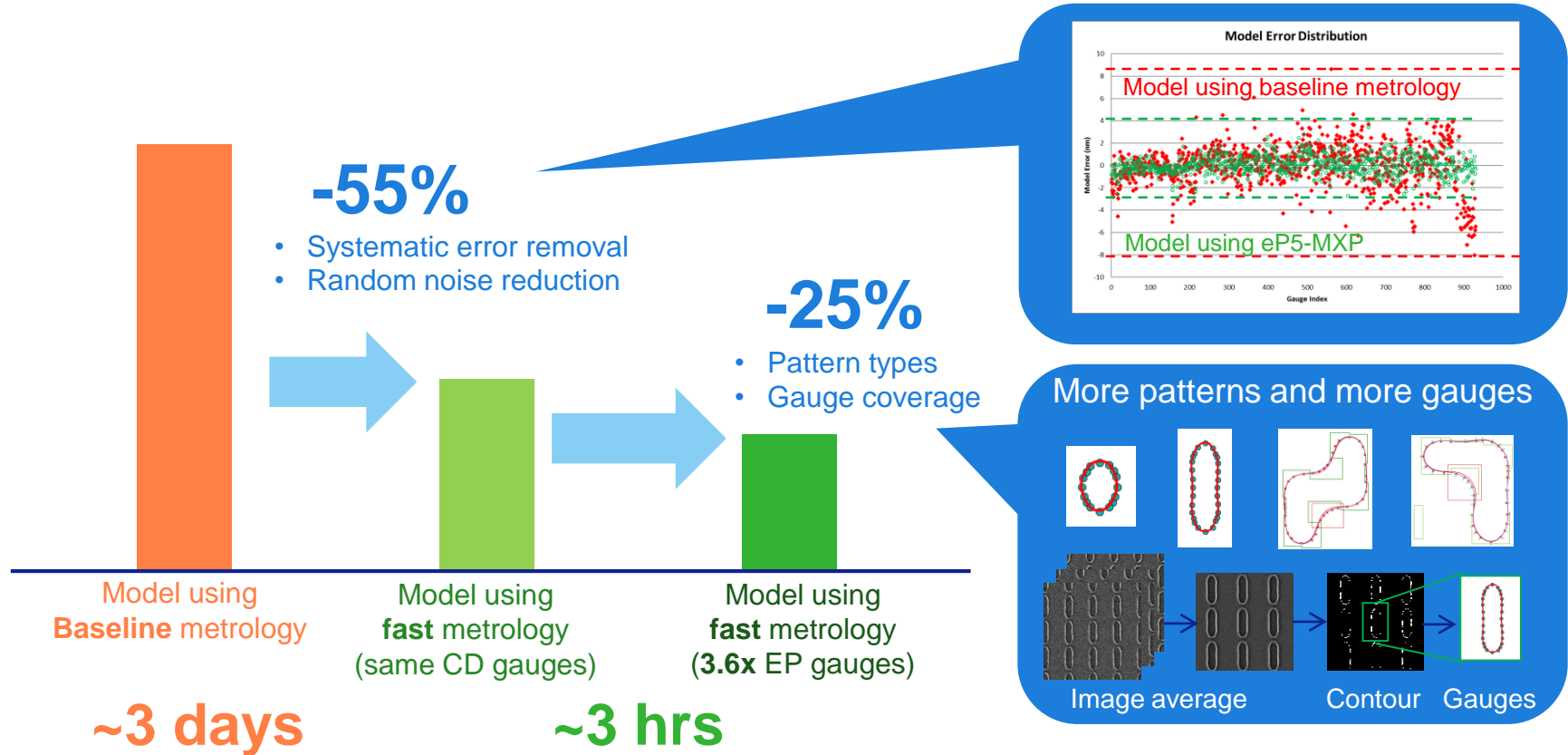


Throughput advantage over CD-SEM



Fast e-beam enables massive metrology sampling

This improves OPC model accuracy and cycle time



Better accuracy of resist models by machine learning

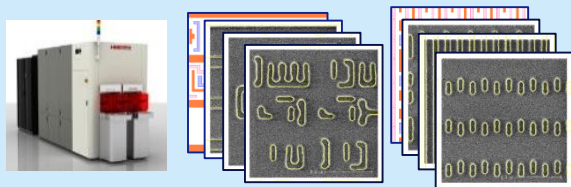
Enabled by fast e-beam metrology and physical based models

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Accuracy

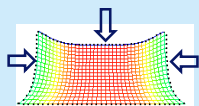
Data-driven **training** based on fitting spec and wafer measurements



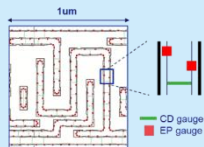
Large volume wafer metrology data,
further enhanced by fast e-beam

Stability

Physical driven **training** using physics based lithography models



Physical Resist
Shrinkage



Data expansion
through simulated
contours

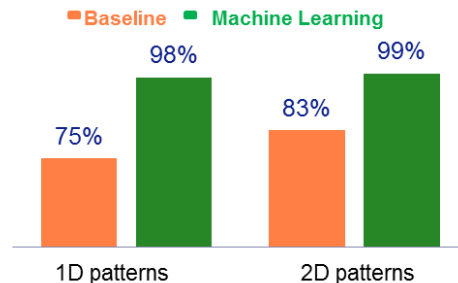
ASML Machine
Learning model



Takes input from
both wafer data and
physics-based litho
models to achieve
better **accuracy**
and retain **stability**

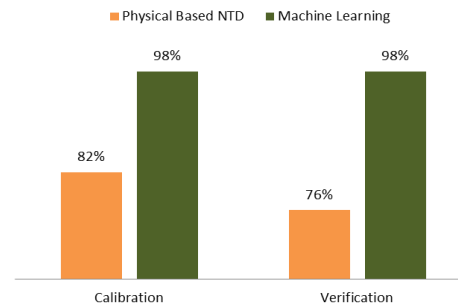
Example 1

Percentage of patterns within accuracy spec



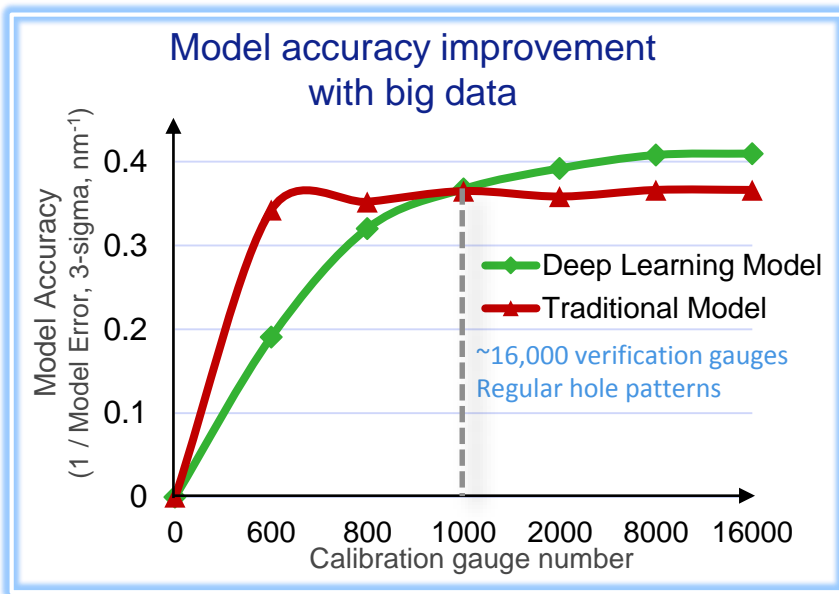
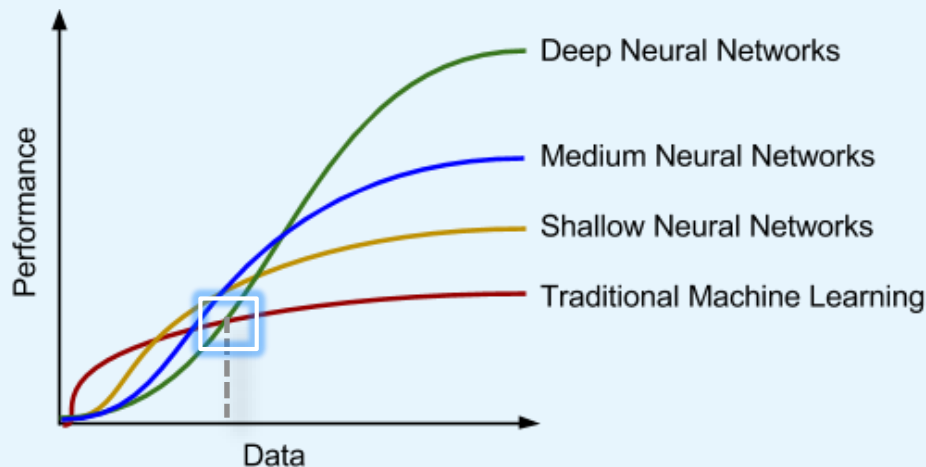
Example 2

Model Accuracy: Percentage of gauges within spec



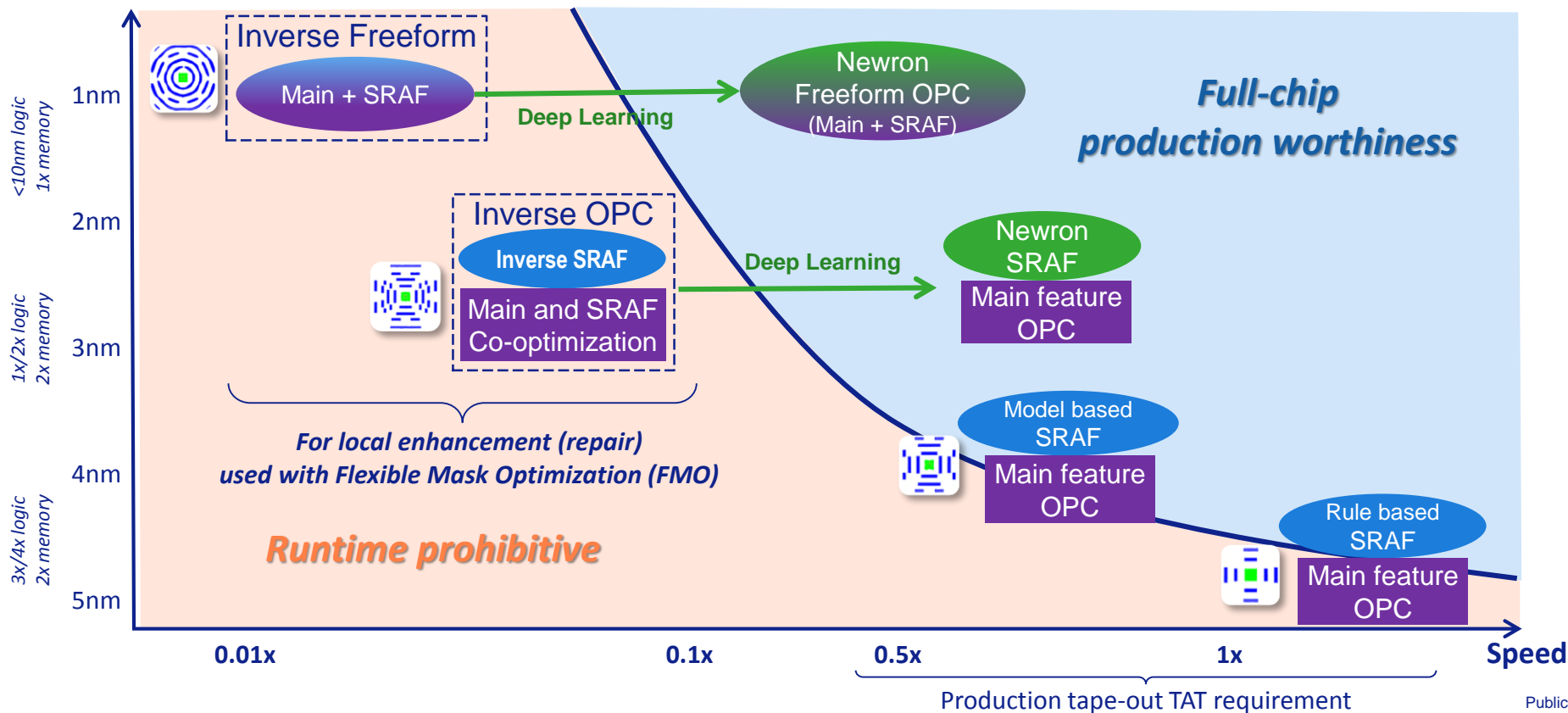
Massive metrology data & deep learning models further improve OPC accuracy in customer case

- Big data improve pattern coverage & enhance model accuracy
- Deep Learning Model has more benefits with big data vs Traditional Model



Deep learning enables full-chip application of inverse SRAF and OPC

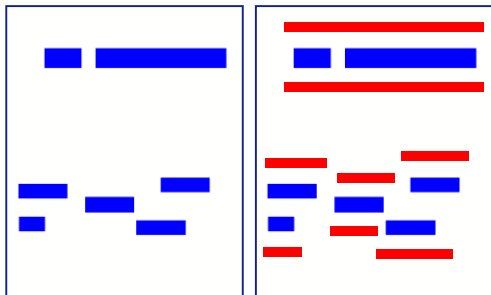
CD Accuracy (through process variations)



Current SRAF placement methods

Targeting different development cost and use scenarios

Rule-based



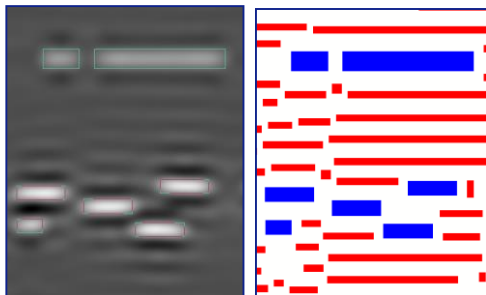
Development

- Time consuming and labor intensive work with trial and error.
- Very fast computation time. Complex 2D layout is a challenge.

Use case

Full chip application, best for simple or 1D pattern.

Model-based (SGM)



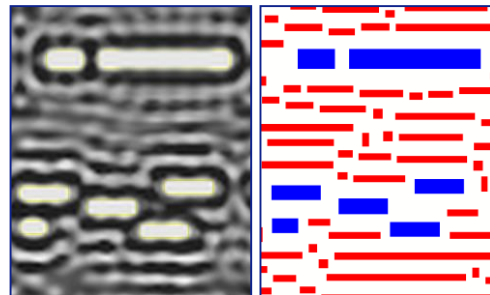
Development

- **SRAF Guidance Map (SGM)** uses gradient-based map calculation method.
- Efficient computation time.

Use case

Full chip application when rule is not good enough.

Model-based (CTM)



Development

- Many iterations to optimize **Continuous Transmission Mask (CTM)** for SRAF extraction.
- Long computation time.

Use case

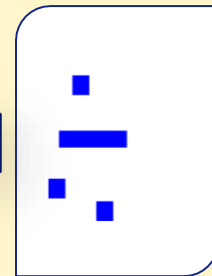
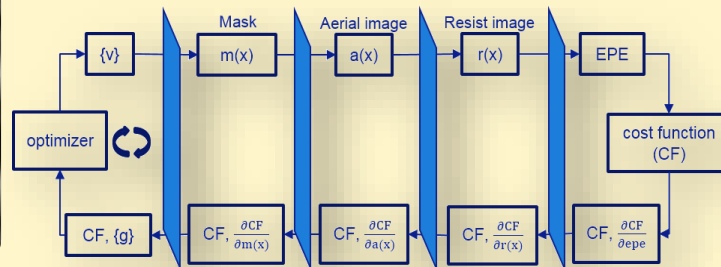
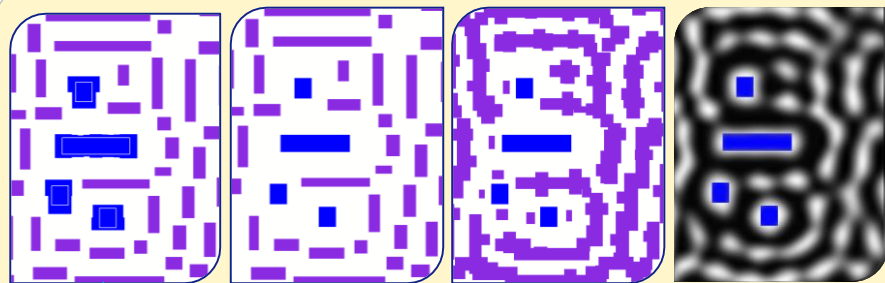
Clip based or local repair, key engine for Brion's inverse lithography solution (Tachyon SMO and iOPC).

DCNN for SRAF placement

Speed up the most accurate SRAF placement method (CTM)

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OPC

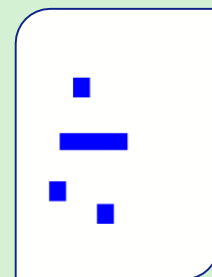
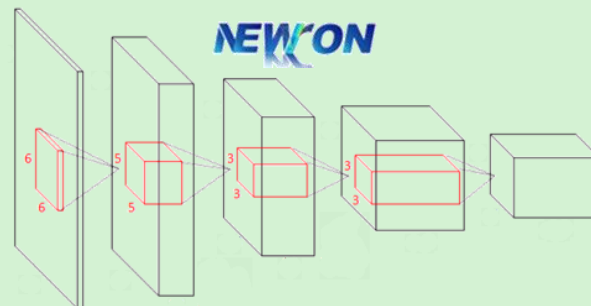
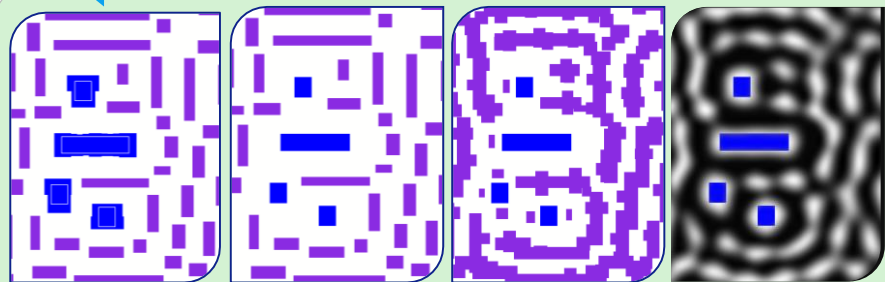
SRAF
Clean-up

SRAF
Extraction

Mask Image

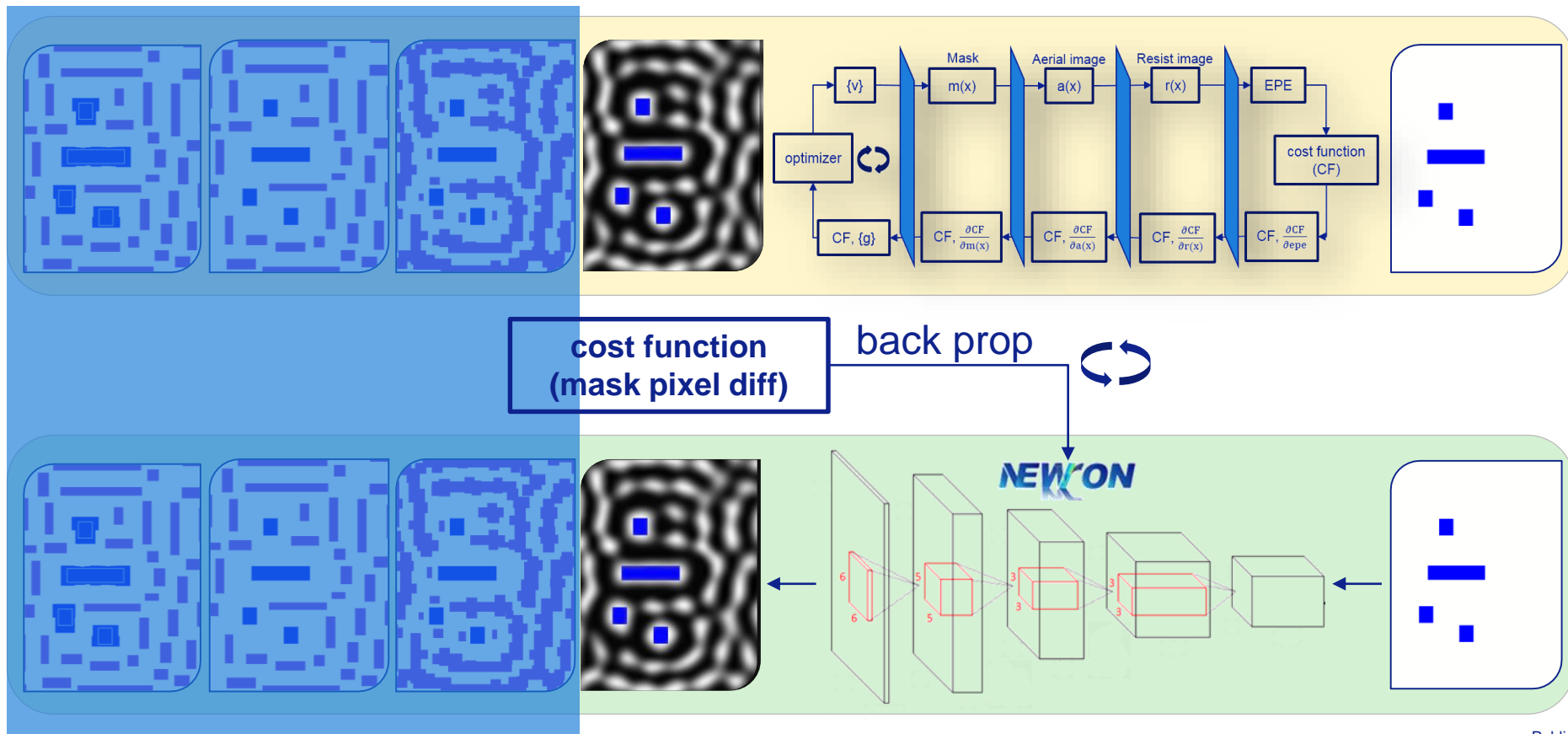
Image-Based Mask Optimization

Target

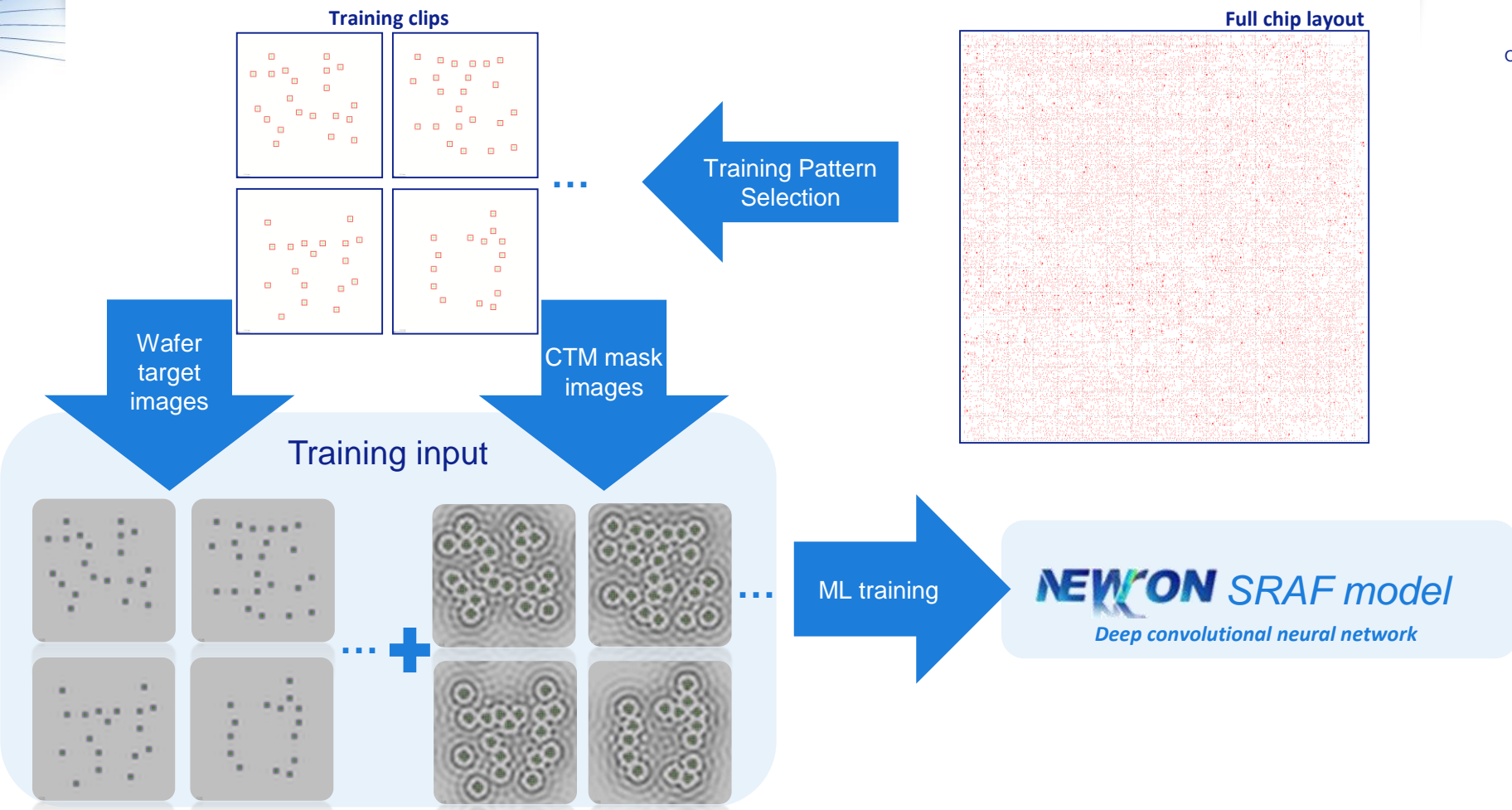


DCNN for SRAF placement: supervised learning

DCNN is trained using sample target and mask images



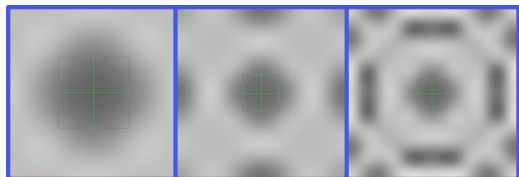
Training a Machine Learning SRAF model



Deep learning assisted SRAF litho performance

- Contact holes through pitch (CD: 54nm, Pitch: 127nm to 700nm)

Ground truth CTM

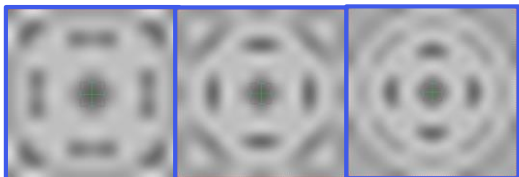
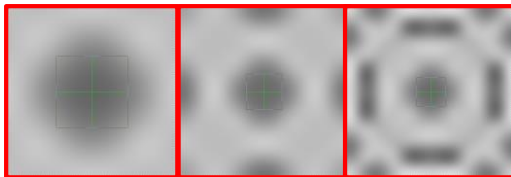


127nm

254nm

318nm

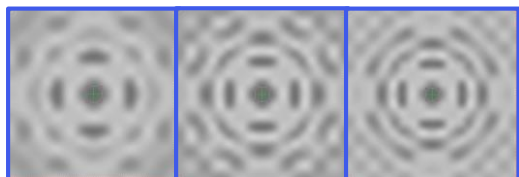
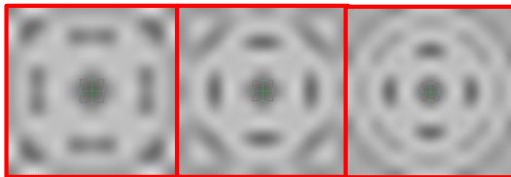
Direct predict - SRAF



382 nm

446nm

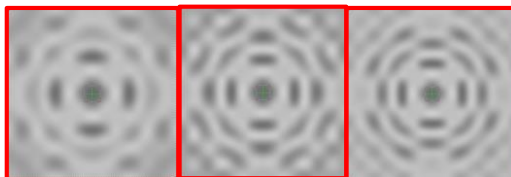
510nm



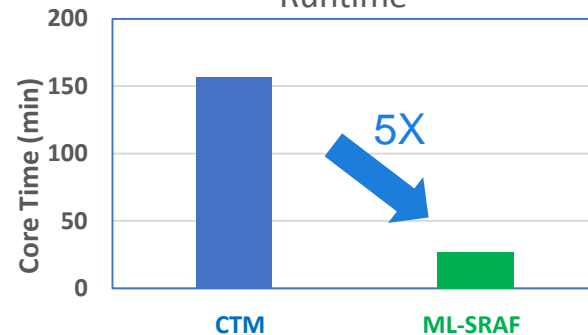
573 nm

637nm

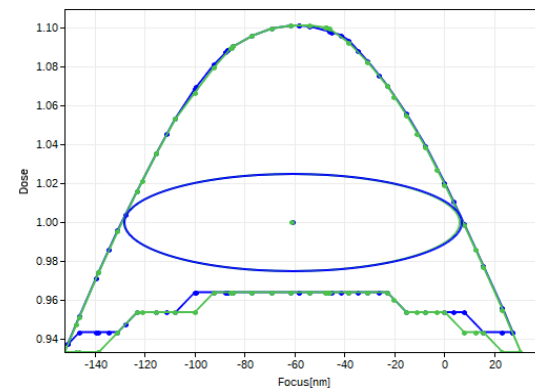
700nm



Runtime



Overlap PW Comparison



Comparison of PV band distribution

Nominal Condition (NC) OPC with different SRAF generations

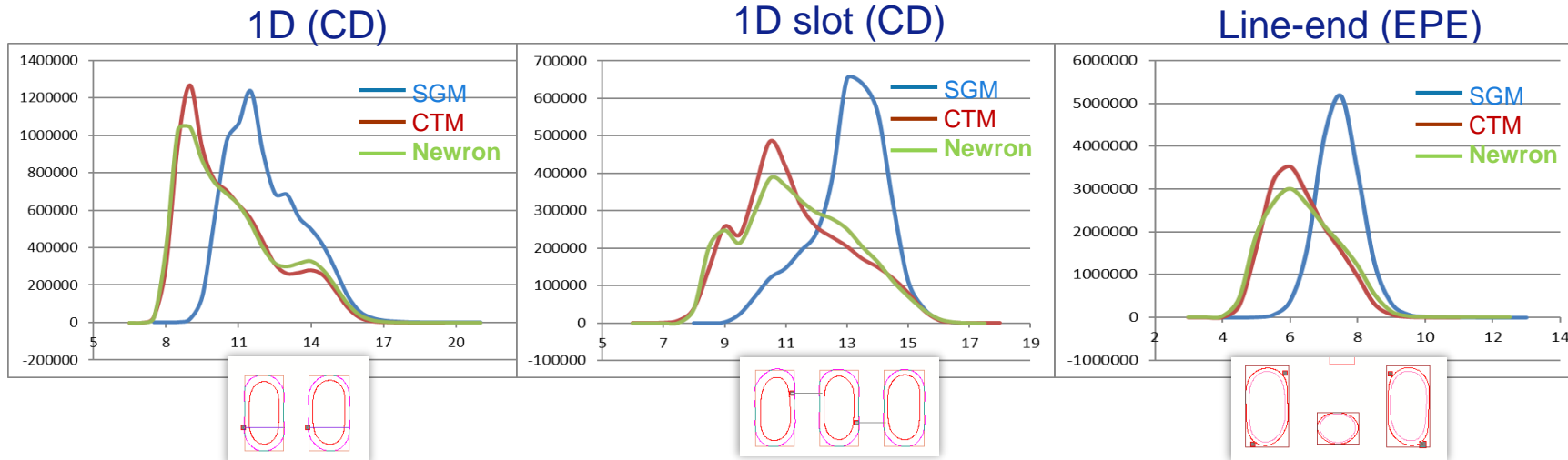
- Design: Advanced node contact layer, 6.5 mm²
- Lithography model: ArFi FlexRay, bright field
- SRAF by SGM/CTM/Newron + nominal condition OPC
- Maximal PV band from wide PW conditions



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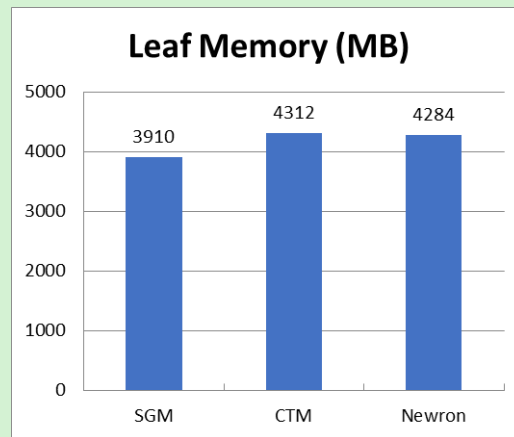
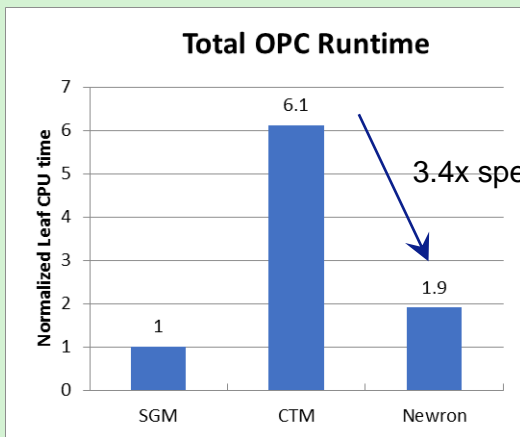
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Statistically, Newron SRAF PV band is smaller than SGM
Newron SRAF follows what it learned from CTM

Runtime and memory

Full Chip OPC job with SRAF generation and Process Window OPC



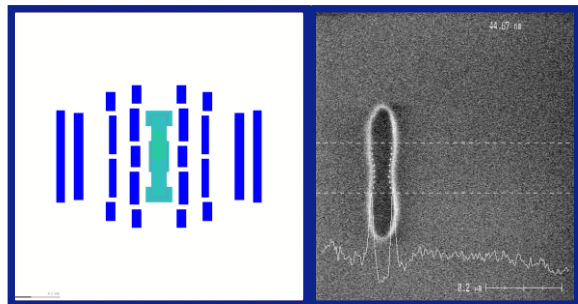
Newron SRAF OPC job is 3.4x faster than CTM in runtime and uses only 9% more memory than baseline SGM.

Wafer validation of Freeform OPC+ on 3D-NAND via layer **ASML**

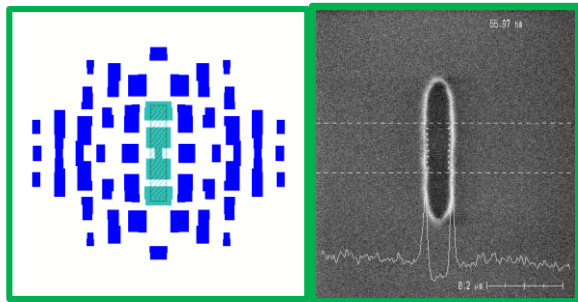
32% improvement in DOF

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Slide 21
October 18, 2018

MO

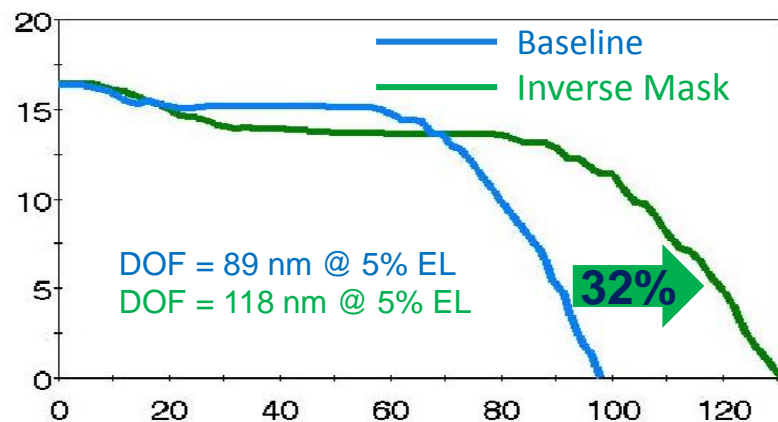


Freeform
OPC



Necking observed with MO is not seen with Freeform OPC

	Simulation DOF @ 5% EL	Wafer DOF @5% EL
Freeform OPC	136nm ↑ 32%	118nm ↑ 32%
Baseline (MO)	103nm	89nm



[SPIE 2018] Sam Liu, "Freeform mask optimization using advanced image based M3D inverse lithography and 3D-NAND full chip OPC application"

Public

Freeform OPC+ delivers accuracy of inverse OPC to full chip

Conventional OPC with MB-SRAF

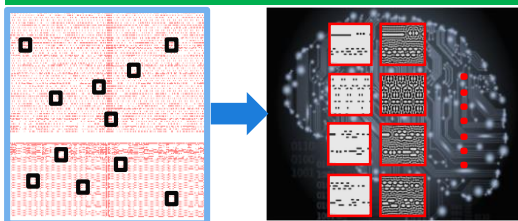
Insufficient accuracy but meets runtime requirements

Freeform OPC+

Best accuracy but too slow for full chip

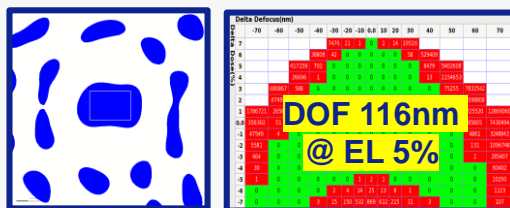
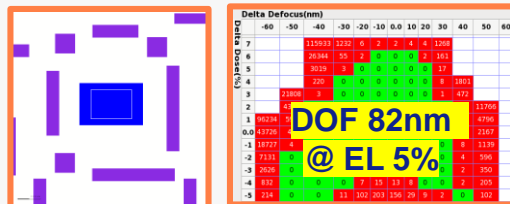
Newron Freeform OPC+

Trained with Inverse on selected patterns

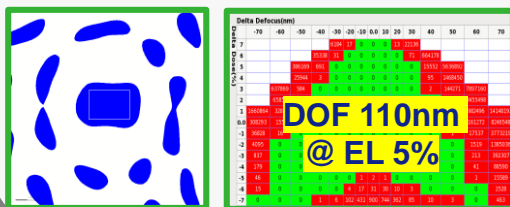


ML Prediction

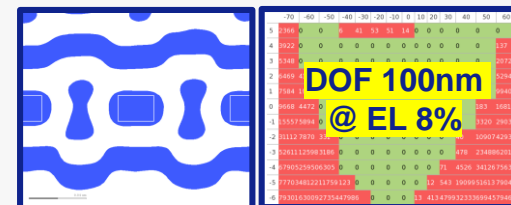
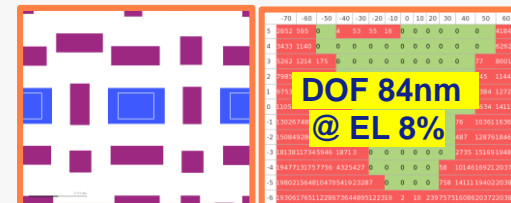
DUV Test case



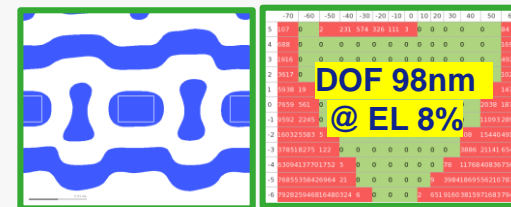
Significant speed-up!



EUV Test case

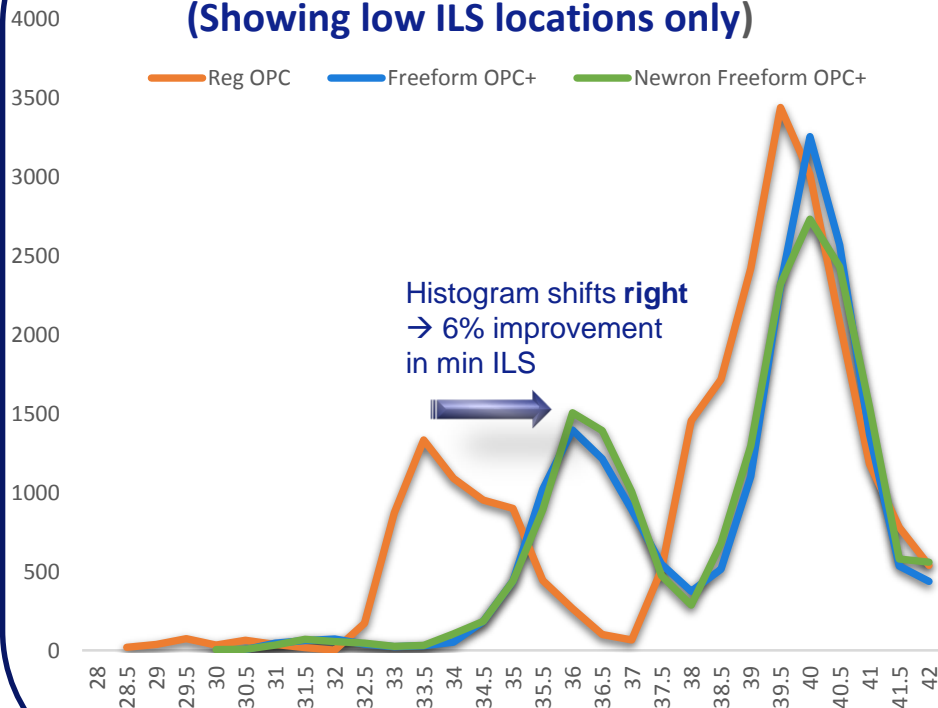


Significant speed-up!

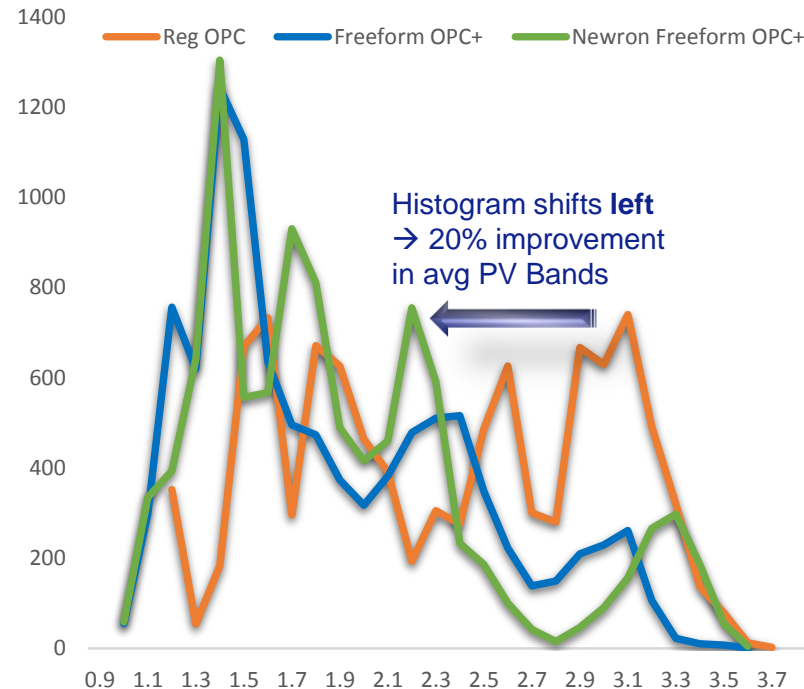


Newron Freeform OPC+ improves ILS and PV Bands, reducing total EPE

ILS Histogram for EUV Test case (Showing low ILS locations only)

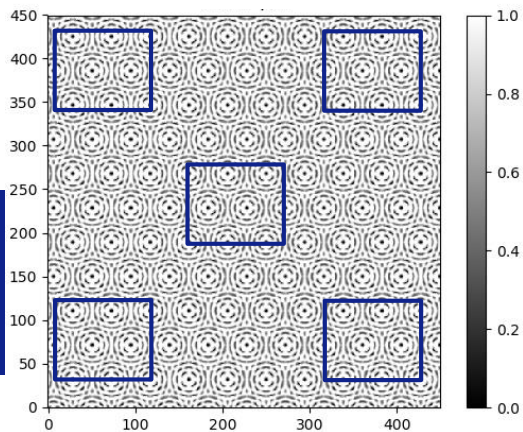


PV Band Histogram for EUV Test case

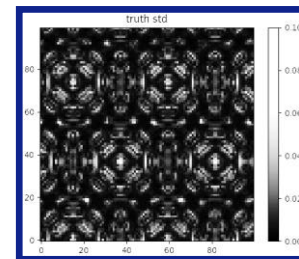
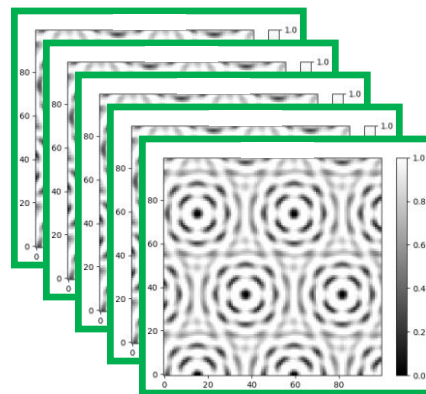
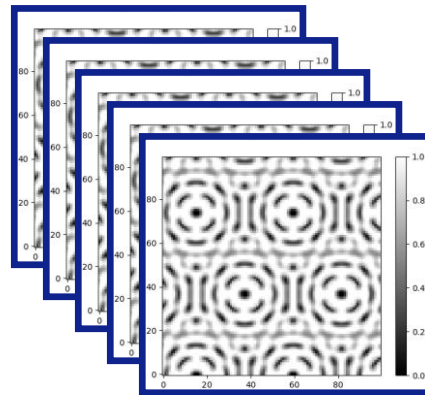
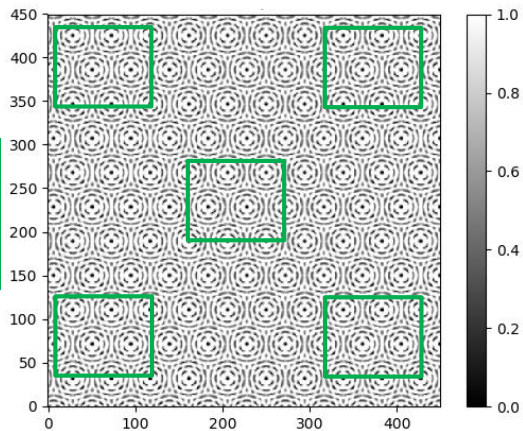


Newron Freeform OPC+ improves image consistency

Freeform
OPC
Ground
Truth

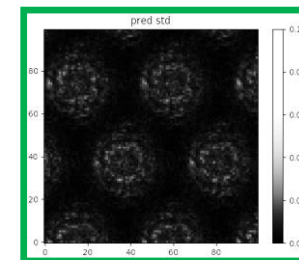


Freeform
OPC
Deep
Learning



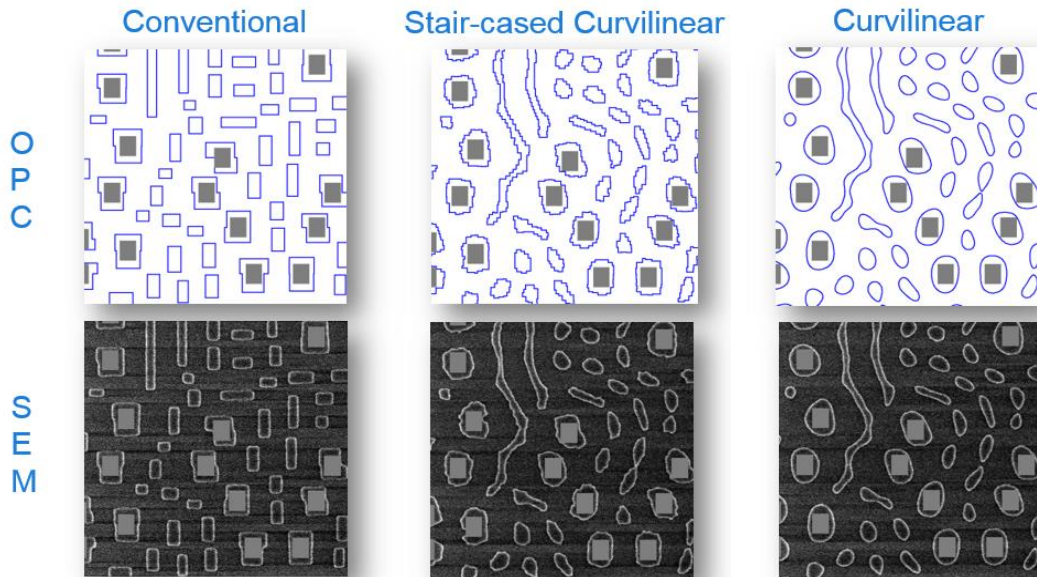
Std = 0.0120

46% improvement in
consistency



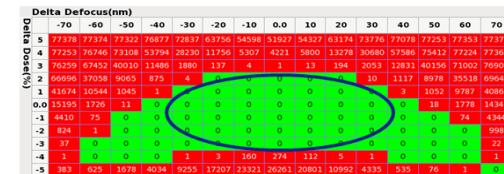
Std = 0.0065

Curvilinear masks can be made using VSB or MBMW

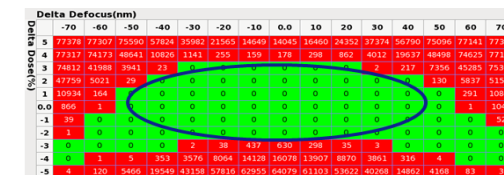


Process window comparison

Conventional mask: DOF=96 nm @ 5% EL



Curvilinear mask: DOF=112 nm @ 5% EL



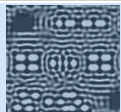
Mask type (DUV)	VSB with conventional fracturing In Hours per Full Field	VSB with freeform fracturing In Hours per Full Field	MBMW In Hours per Full Field
Conventional mask	12.6	-	12.4 (30 v/um ²)
Stair-cased curvilinear mask	95.0	-	12.4 (169 v/um ²)
Curvilinear mask	757	79	12.4 (164 v/um ²)

Spence et al., "Manufacturing challenges for curvilinear masks", Proc. SPIE 10451, Photomask Technology, 1045104

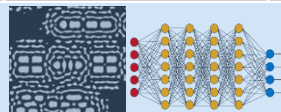
Leverage confluence of new technologies to meet OPC technology and cost requirements

2016	2017	2018	2019	2020	2021
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Inverse OPC (CTM)



Inverse OPC (CTM+) Deep Learning Inverse



Inverse with phase control Hardware Accel. (tentative)



Intel Xeon Processor E5 v4



Skylake

Intel DL Boost



Cascade Lake



Cooper Lake

14 → 10 nm



Ice Lake



Intel Xeon Scalable processor with integrated FPGA



Nervana Spring Crest



Pascal



Volta

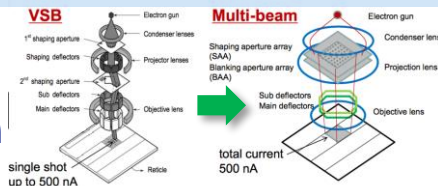


Turing



Next Gen?

Mask writer & inspection



Mask inspection available

Mask making infrastructure is ready for inverse OPC & curvi-linear masks

Multi-beam Mask Writer available

Data, algorithms, and applications for patterning solutions **ASML**

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Oct 2018

Lithography scanner with advanced control capability



Etch and deposition tools

Applications
Mask, Litho, & Etch
Pattern Fidelity Control

Algorithms
Physical Models,
Inverse Optimization,
Machine Learning

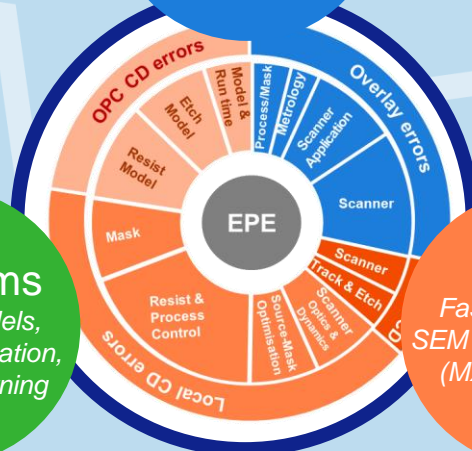
Data
Fast SEM (eP5),
SEM data processing
(MXP), other fab
equipment



Computational lithography and metrology



Optical and e-beam metrology



The image features the ASML logo in a bold, dark blue, sans-serif font. The logo is positioned on the left side of the frame. The background is a light blue gradient with abstract, flowing white lines that sweep across the lower half of the image, creating a sense of motion and modernity.

ASML