Coater / Developer System Latest Technology

October 17th, 2019

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Clean Track Marketing
Tokyo Electron Limited

Outline

1. EUV technology improvement work
   - In film particle reduction
   - CDU improvement
   - Pattern collapse reduction

2. Coater/Developer system latest technology
   - Rapid detection
   - Autonomous control

3. Summary

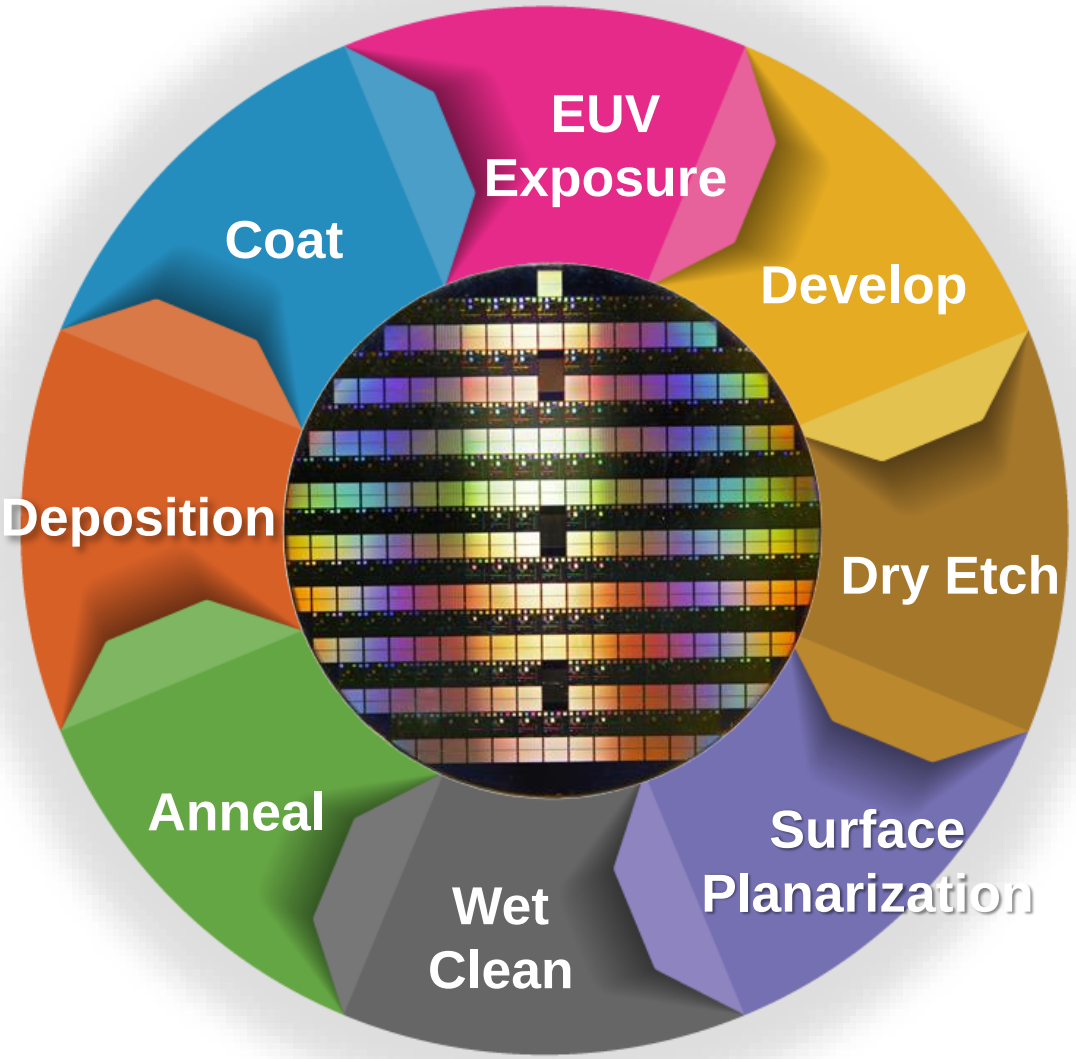
EUV technology improvement work

EUV patterning performance improvement using equipment set

Coater/Developers

Single Wafer Deposition System

Thermal Processing System



Plasma Etch System

Cleaning System

CLEAN TRACK™ LITHIUS Pro™ Z

Coater/Developer

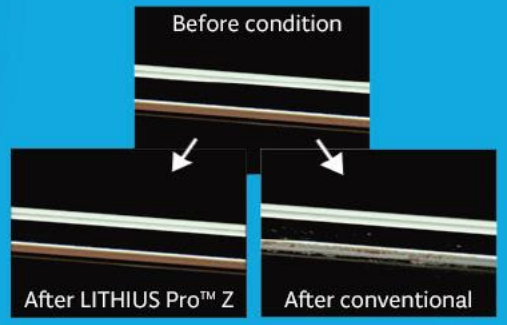
Features

- Low particle wafer transfer system
- Improved Overall Equipment Efficiency (OEE) for litho cells
- Reduced Cost of Consumables (CoC) and energy usage

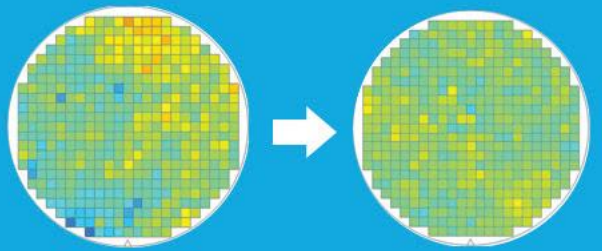
Applications

- EUV, immersion, ArF, KrF, i-line
- 200mm and 300mm wafers

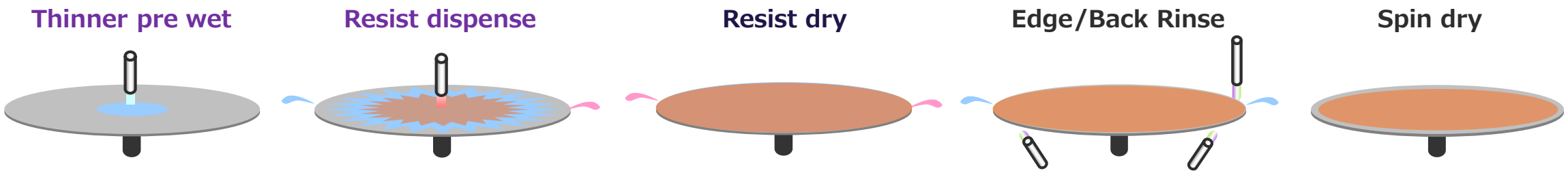
Contact area comparison
(after 500 transfers)

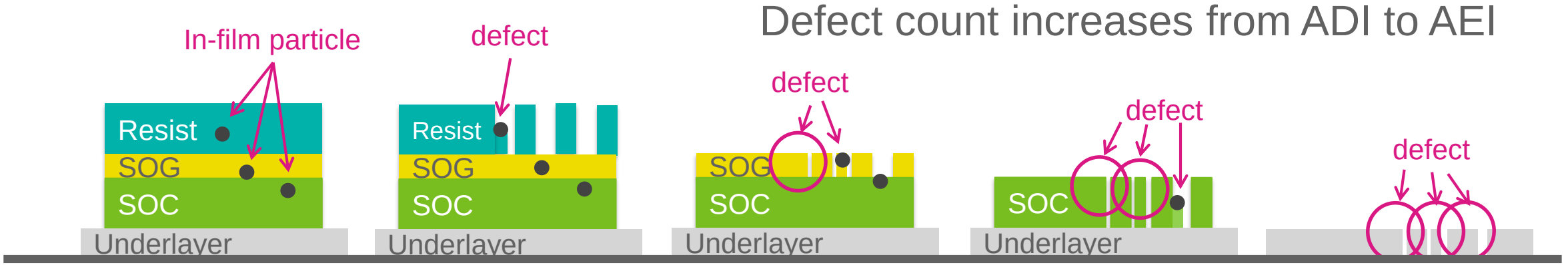


Improved CDU control



Importance of in-film particle reduction





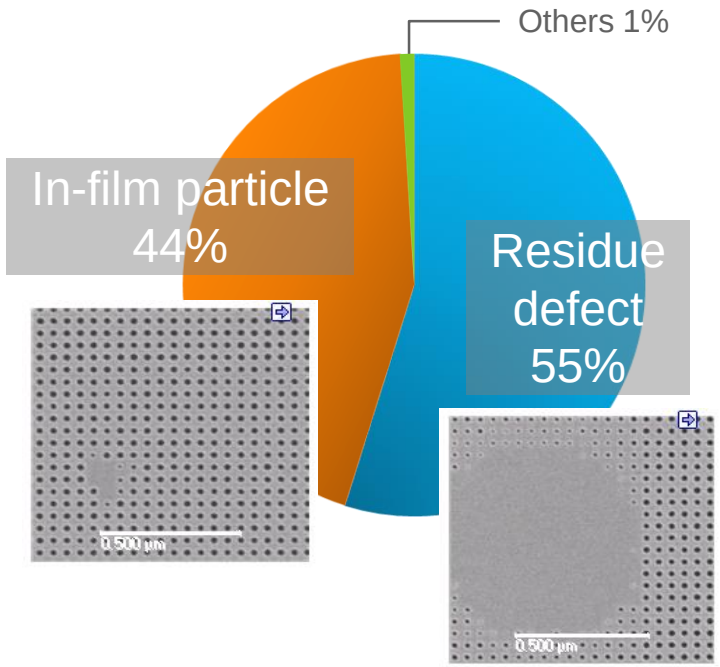
In-film particle reduction is key to improve defect density

EUV defect budget analysis: 24 nm HP CH

After development inspection (ADI)

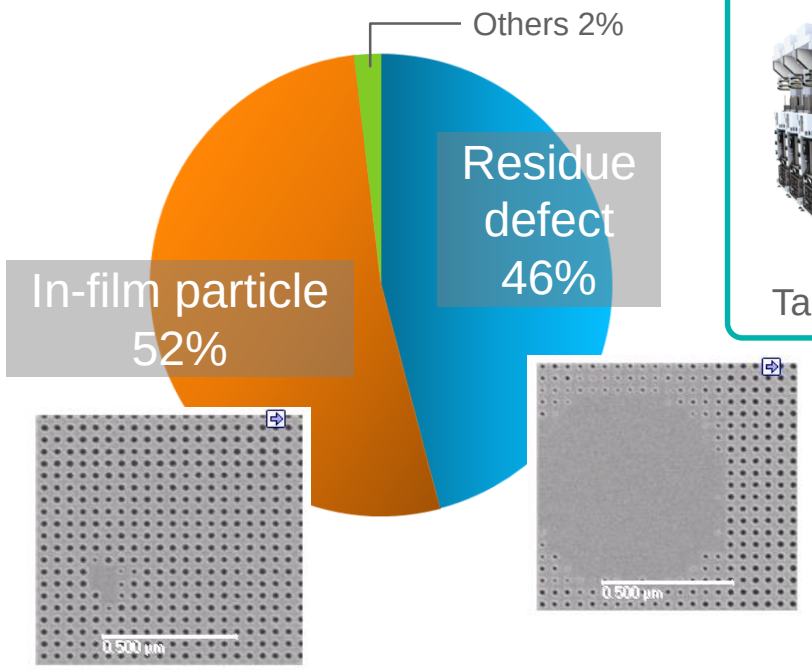
ADI Defect Budget

CLEAN TRACK™ LITHIUS Pro™ Z-EUV and NXE:3300



After etch inspection (AEI)

AEI Defect Budget



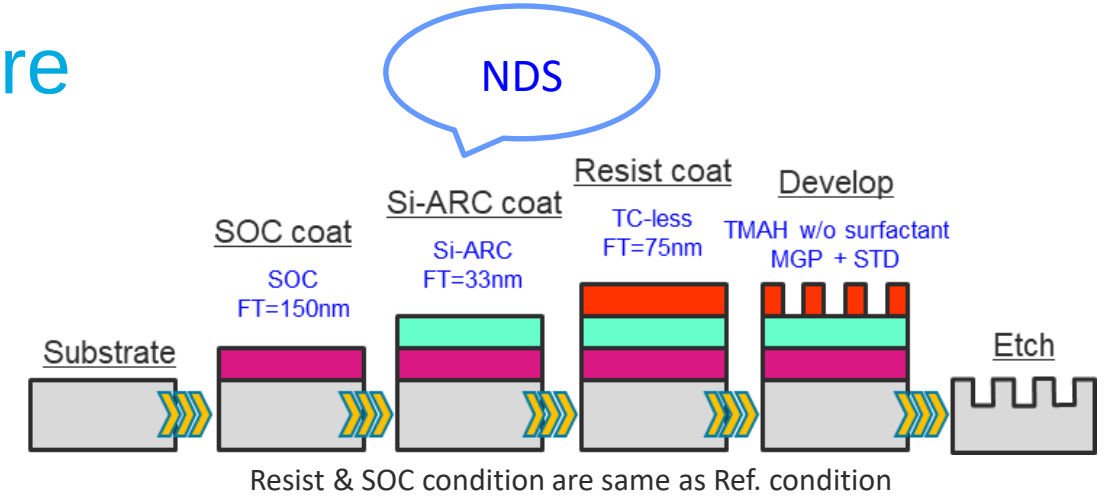
Tactras™ for etch

Residue defect and in-film particle are the dominant before and after etching

In-film particle reduction measure

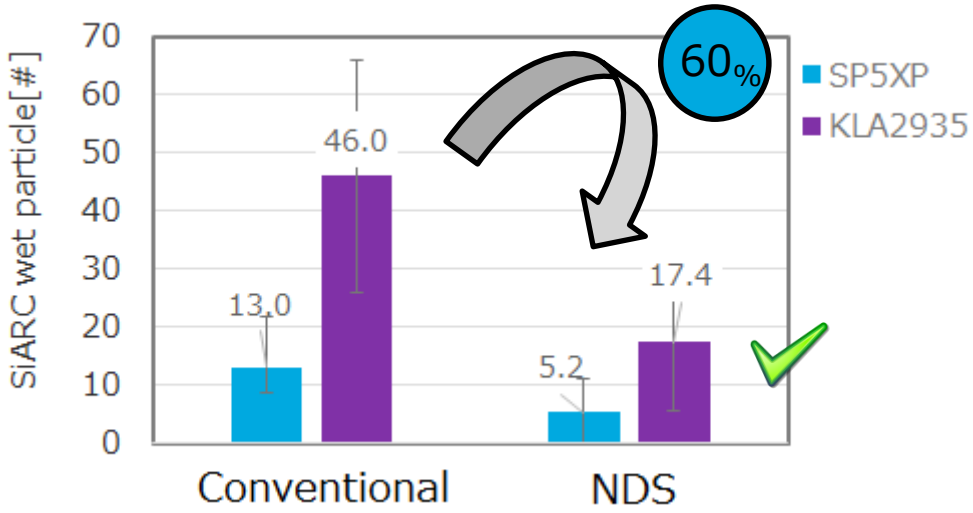
■ Test Condition

Pattern : 45nm LS 1:1
Filter : HDPE 2nm for Si-ARC
Track : LITHIUS Pro™ Z
Pump for Si-ARC : Conventional, New dispense system (NDS)
Metric : Wet particle & AEI TEST Scheme

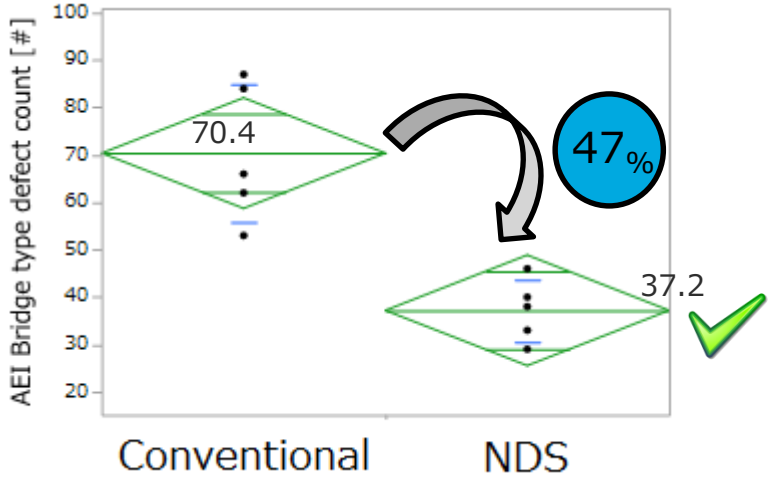


Resist & SOC condition are same as Ref. condition

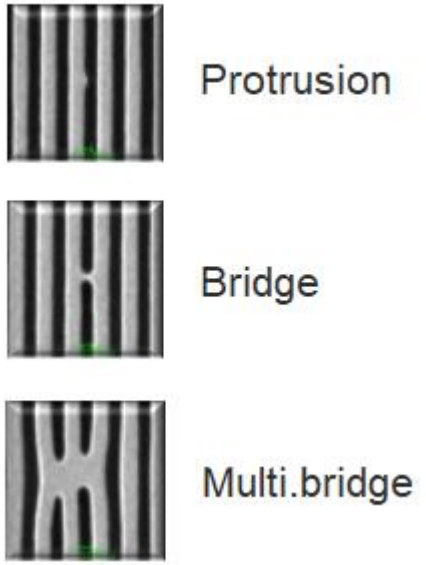
■ Si-ARC wet particle



■ AEI Bridge type defect



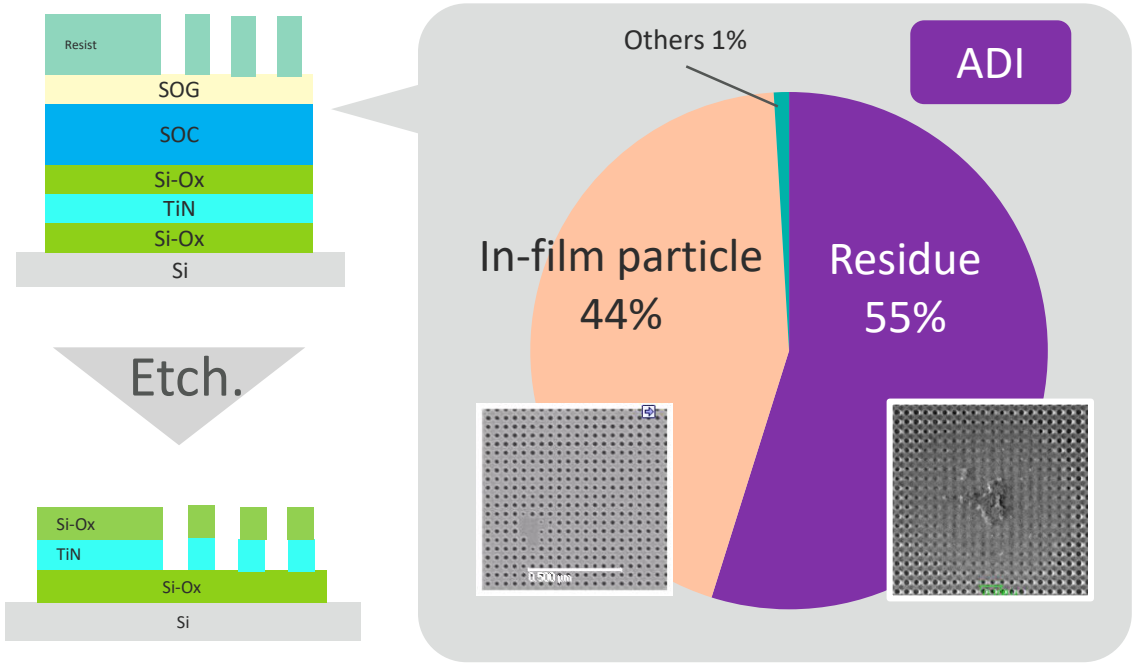
Bridge type mode

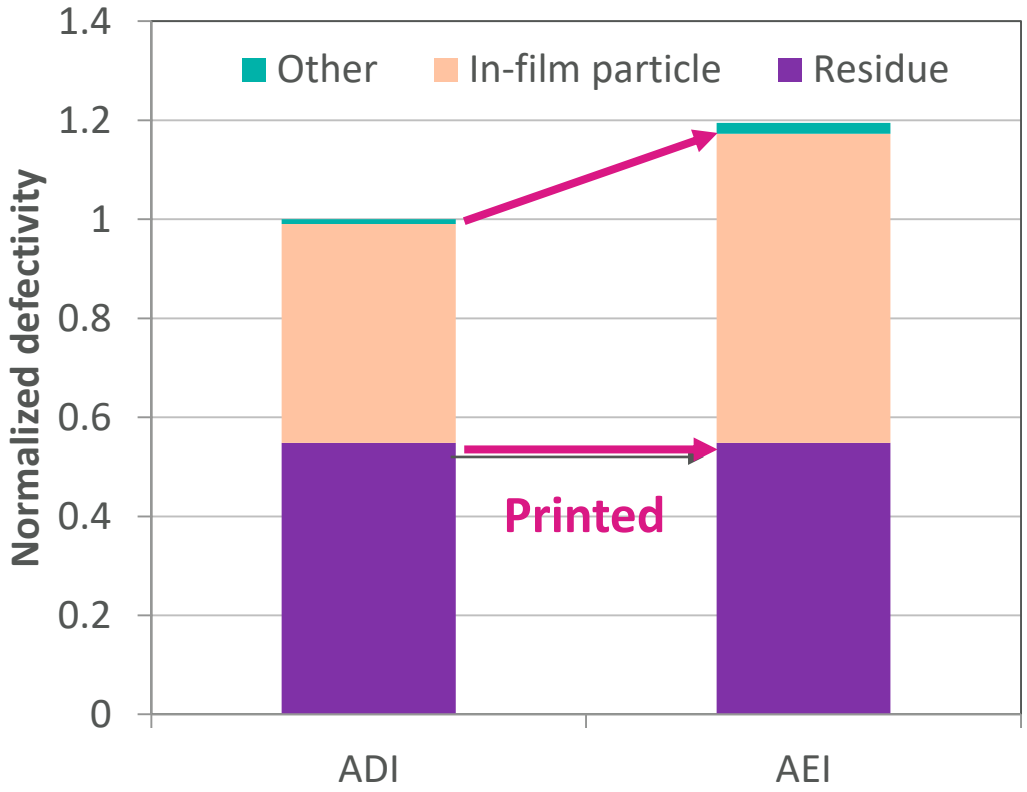


NDS shows better performance for wet particles/AEI defects than conventional pump

Residue defect printability to AEI

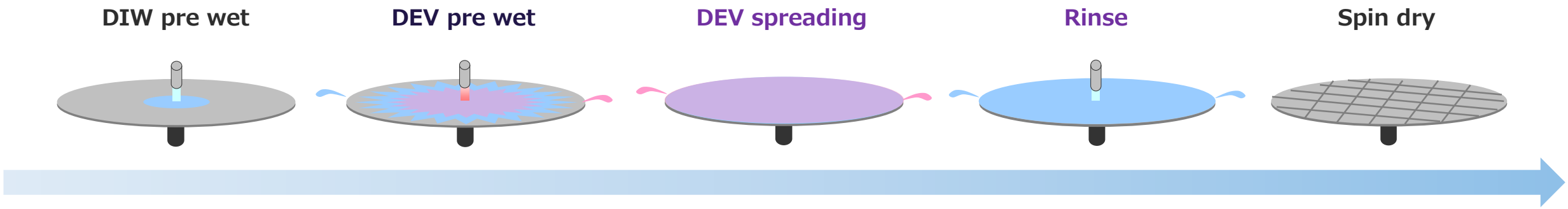
EUV Thru-Etch Defectivity on 24nm Contacts



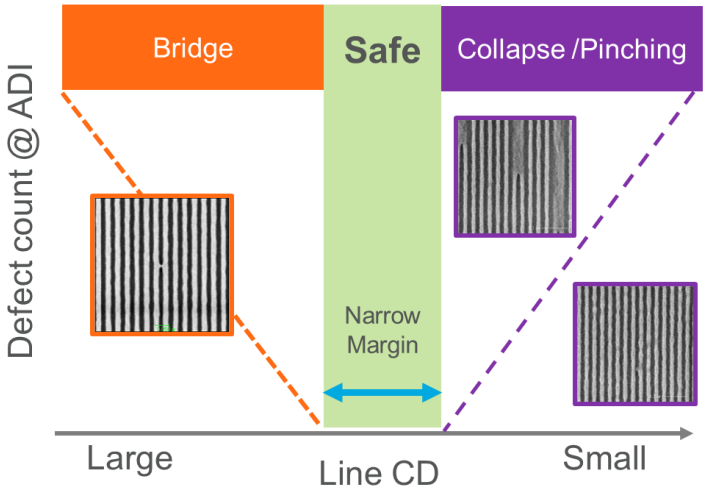


Residue defect is likely printed 100% through ADI to AEI → Need control

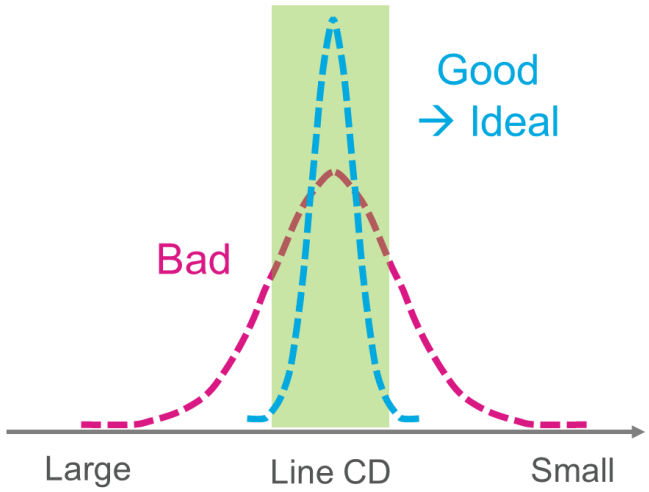
Importance of defect control in developer



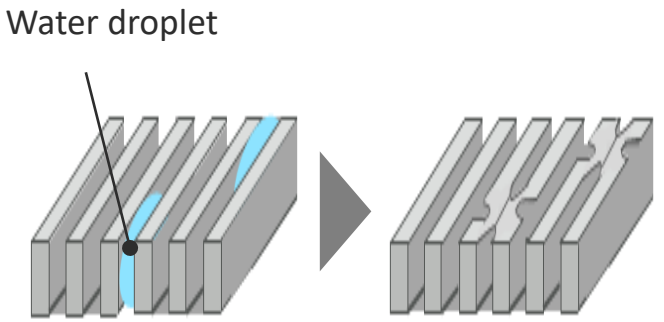
EUV Stochastic Failure Behavior

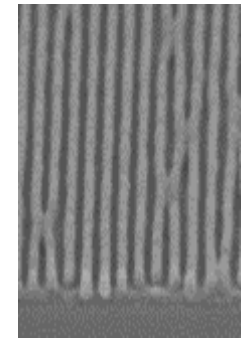


Within Wafer CD Uniformity



Residual Droplet Impact





18nm LS
Pattern Collapse

Experimental conditions

- Coater/Developer: CLEAN TRACK™ LITHIUS Pro™ Z-EUV
- EUV Scanner: ASML NXE:3300
- Etching tool: Tactras™
- Inspection tools:

  Defectivity measurement: KLA2935 from KLA-Tencor

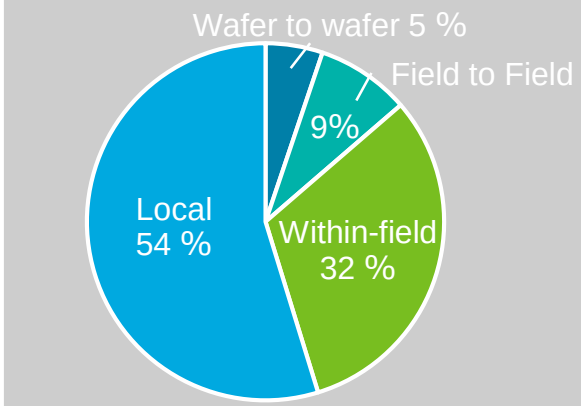
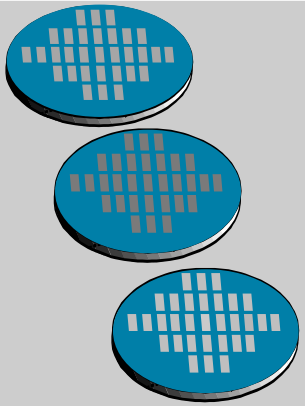
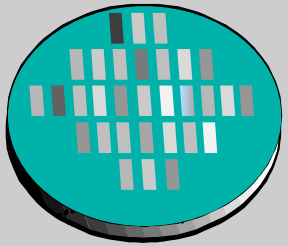
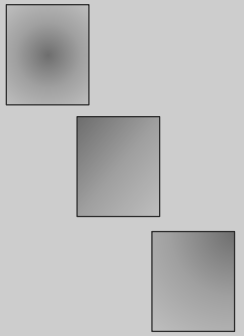
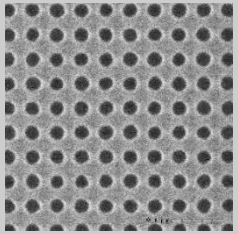
  Defect review: SEMVision G6 from Applied Materials

  CD measurement: CG6300 from Hitachi High Technologies
- Materials and Film Layer

CLEAN TRACK™
LITHIUS Pro™ Z-EUV

Tactras™

Components and probable contributors for CDU

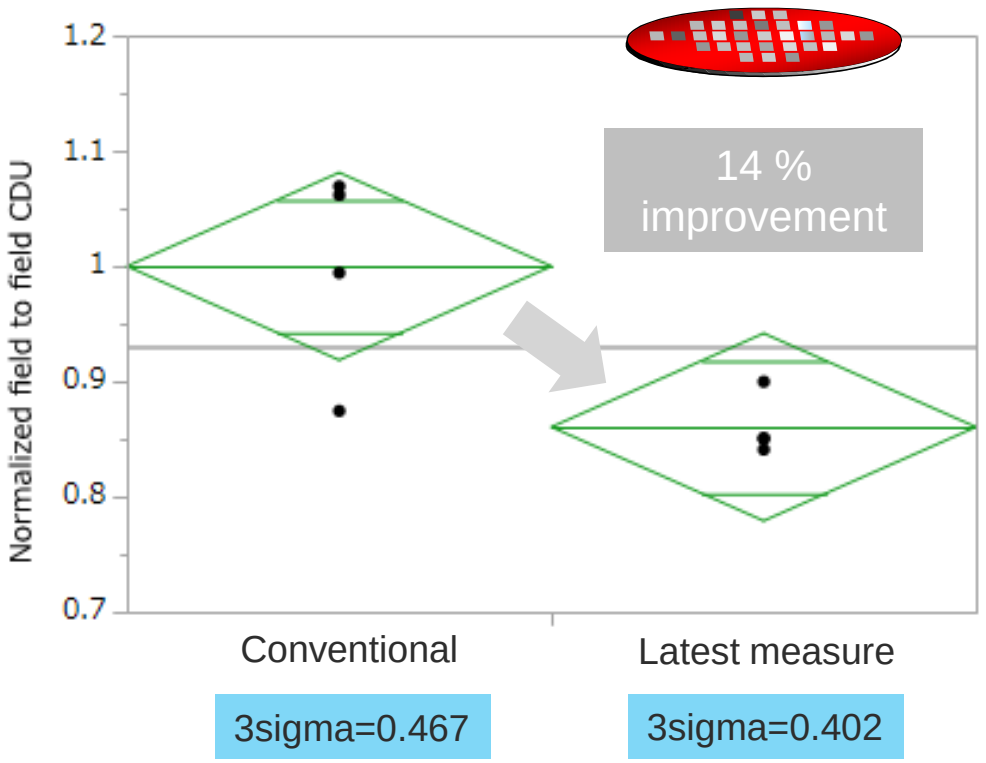
CDU Components		Wafer to wafer	Field to field	Within field	Local CDU
					
Probable contributors	Scanner	✓ [3]	✓ [3]	✓ [3]	✓ [3]
	Mask			✓	✓
	Material				✓
	Coater/developer	✓	✓	✓	✓

Coater/developer as well as scanner, mask, and material are probable contributors to CD variation.
→For Field to field and Within field CDU improvement, developer process was optimized and compared with conventional condition.

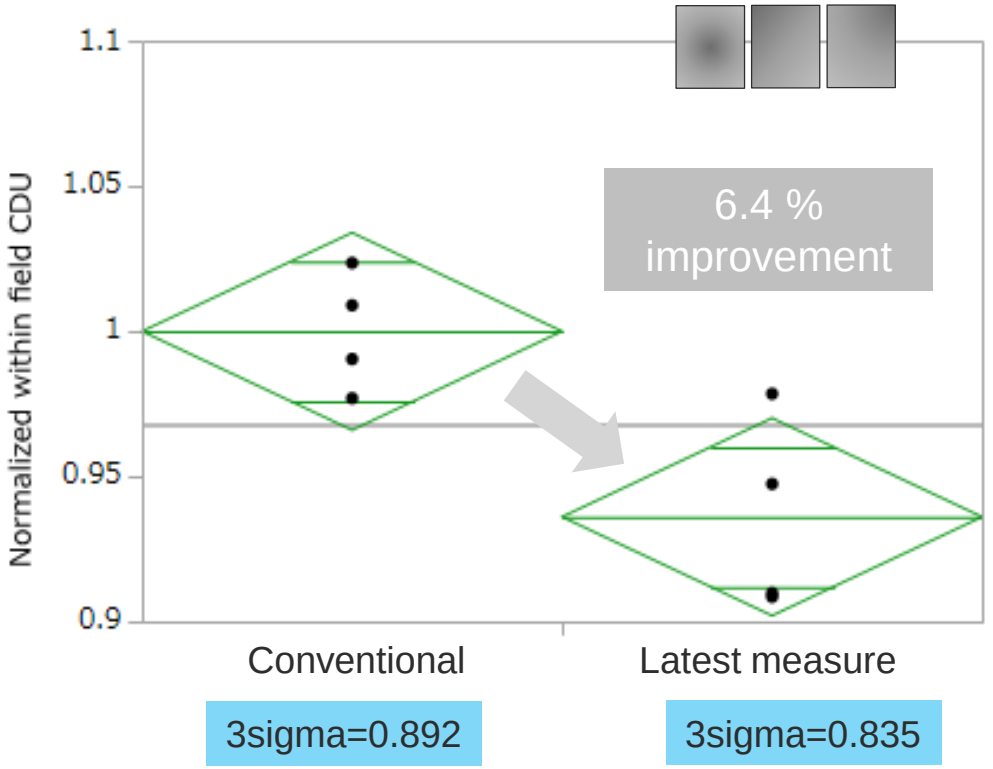
[3] Lieve Van Look *et. al.*, “Optimization and stability of CD variability in pitch 40 nm contact holes on NXE:3300,” Proc. SPIE 10809-0M (2018).

Field to Field and Within field CDU improvement

- Field to field CDU on contact hole 24 nm HP



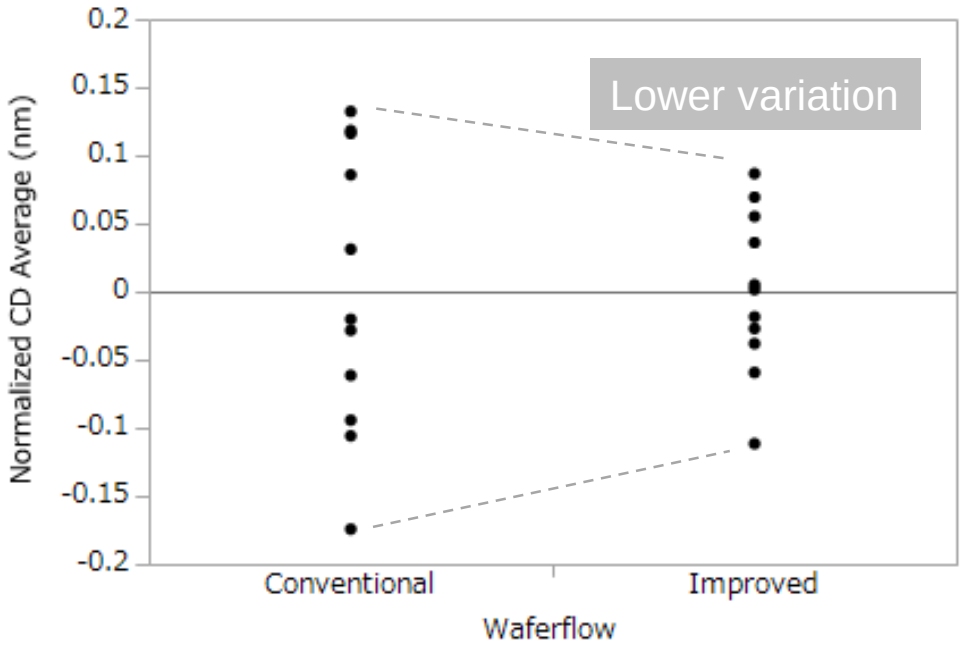
- Within field CDU on contact hole 24 nm HP

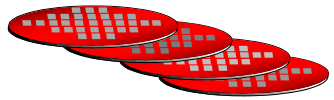


- Latest measure improves both field to field and within field CDU significantly

Wafer to Wafer CDU improvement

Wafer to wafer CD uniformity with batch processing: P = 0.044



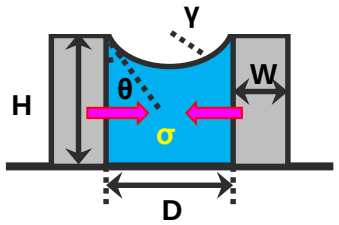


3Sigma = 0.281 nm 3Sigma = 0.178 nm

Wafer to wafer CD variation has been improved by 36 % by track process optimization.

How to control pattern collapse

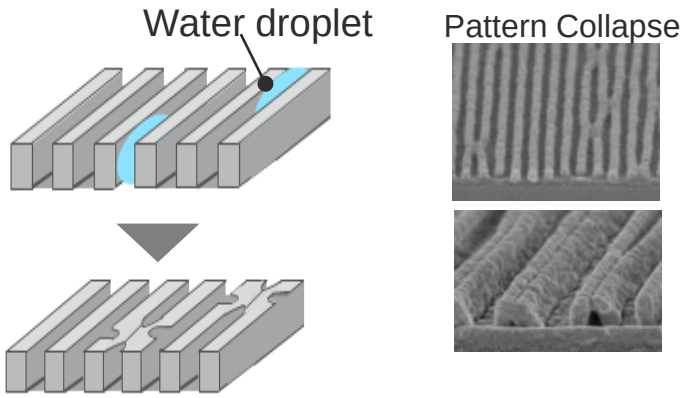
Capillary force



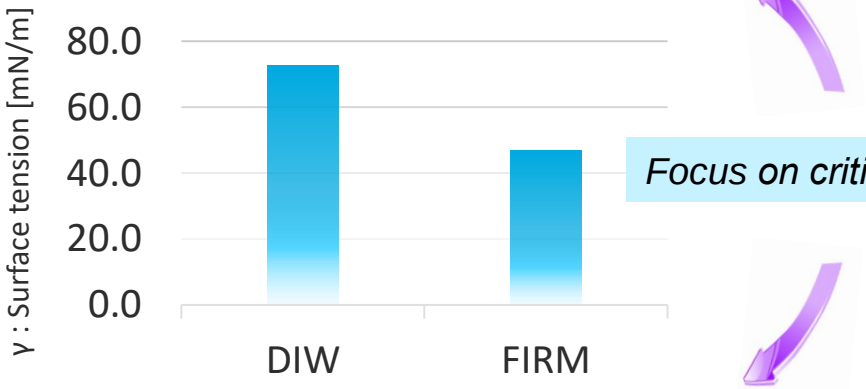
$$\sigma_{resist} > \frac{6\gamma\cos\theta}{D}\left(\frac{H}{W}\right)$$

σ ; The maximum stress which works to pattern
γ ; Surface tension of rinse
θ ; Contact angle
H ; Height of pattern
D ; Pitch of pattern
W ; Width of pattern
H/W ; Aspect ratio

Water droplet

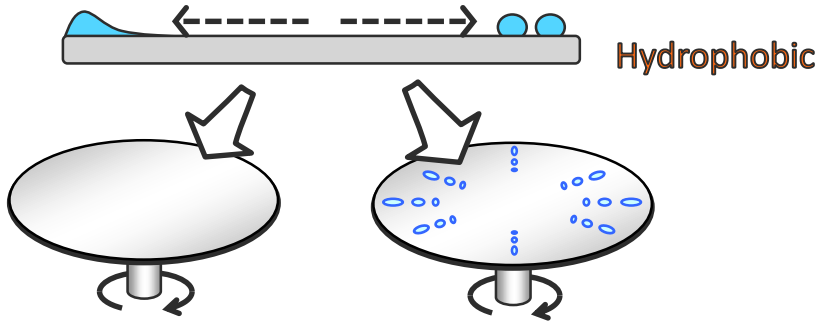


Focal point (1) Low surface tension



Focus on critical stress (γcosθ) reduction

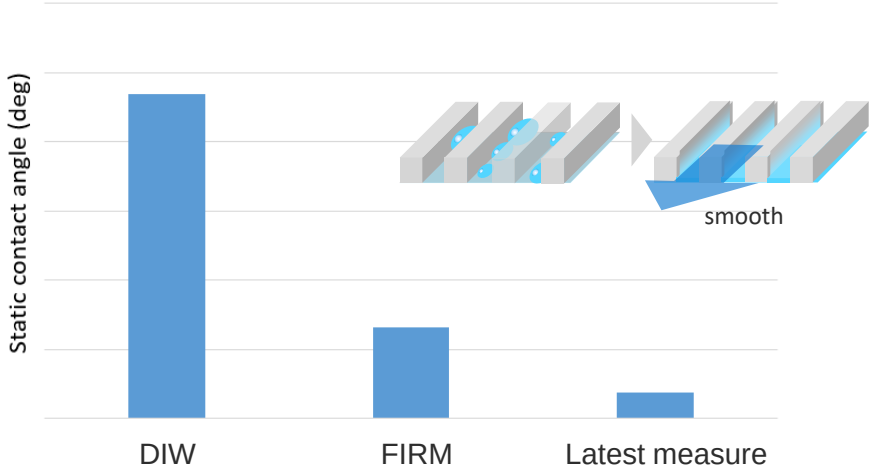
Focal point (2) Surface contact angle optimization



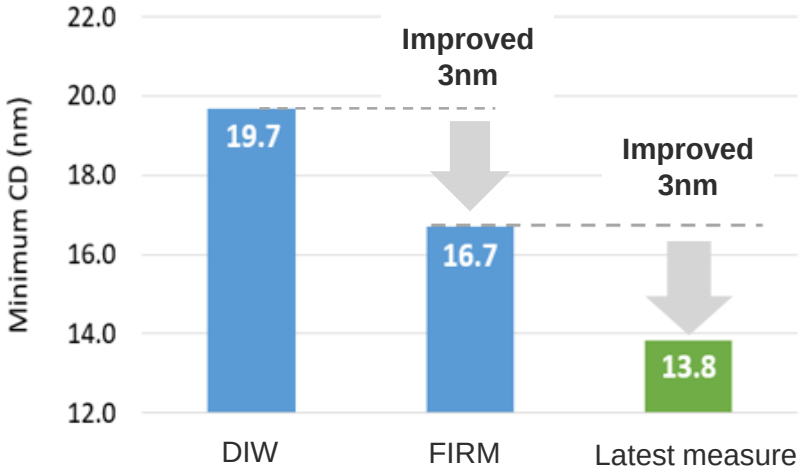
Higher contact angle leads to many droplets generation during rinse process.
→ Need contact angle optimization

Optimized rinse performance

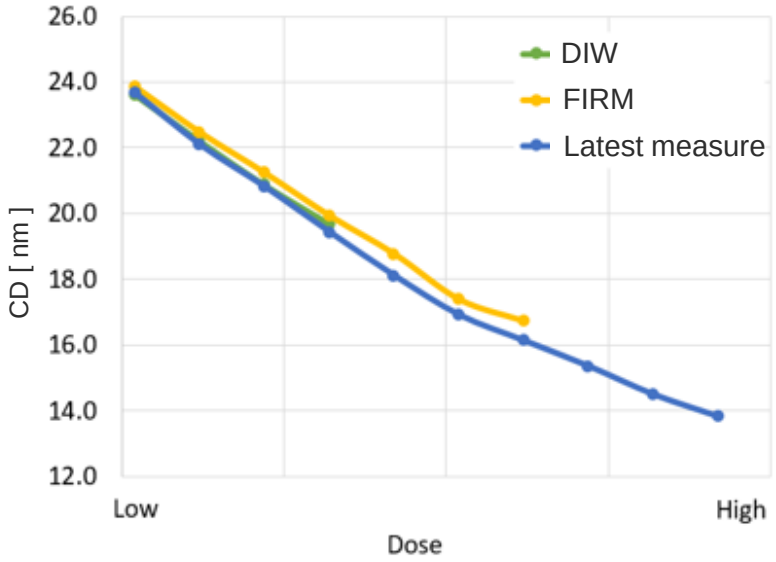
Contact angle optimization result

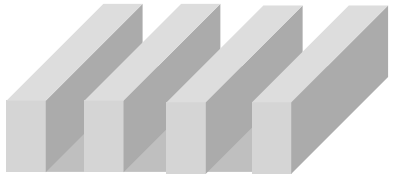


Minimum CD with no collapse

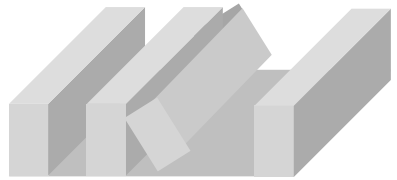


CD without pattern collapse





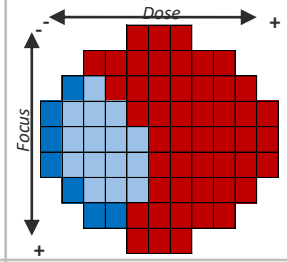
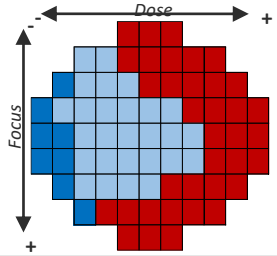
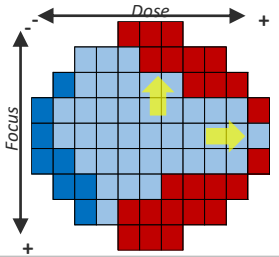
Good

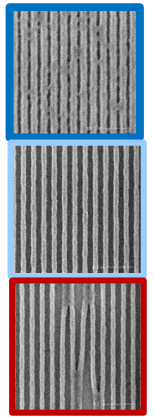


Collapse

Process window and resist pattern height

- **Process Window**

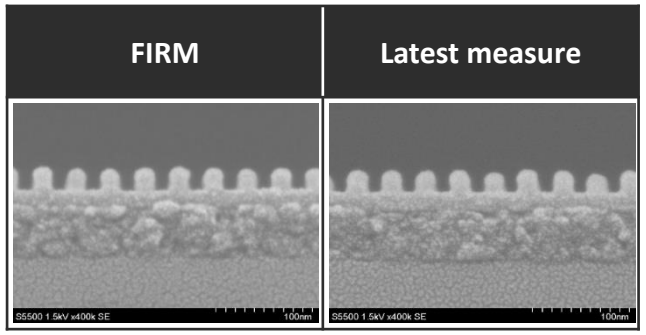
Rinse	DIW	FIRM	Latest measure
			
# of shot with no collapse	15	27	39

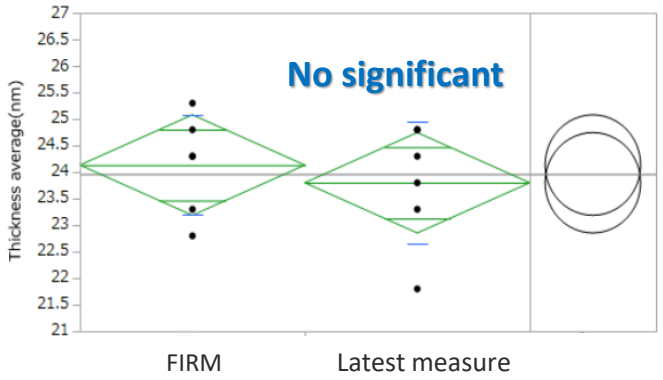


Bridge

Collapse

- **Pattern height (X-SEM inspection)**

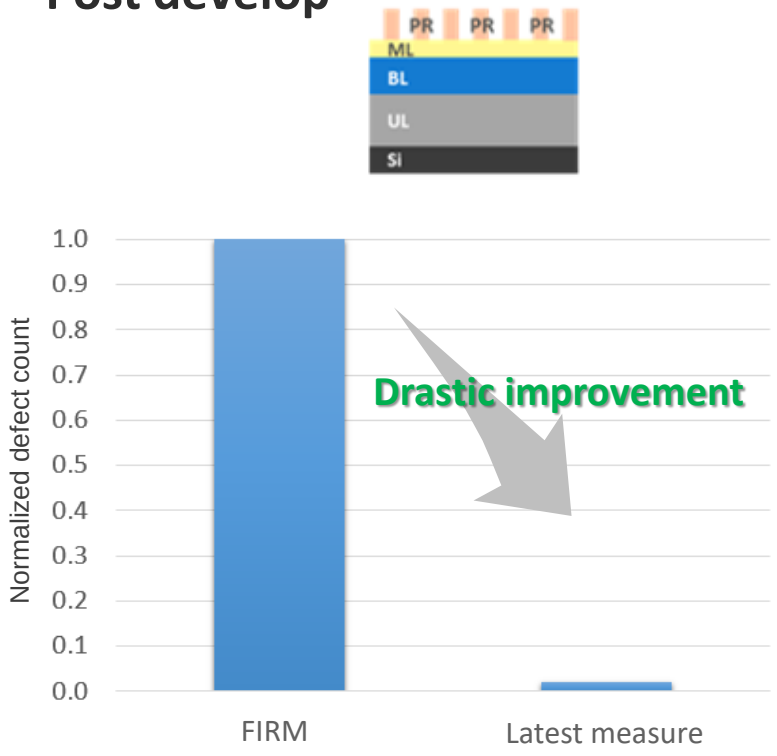




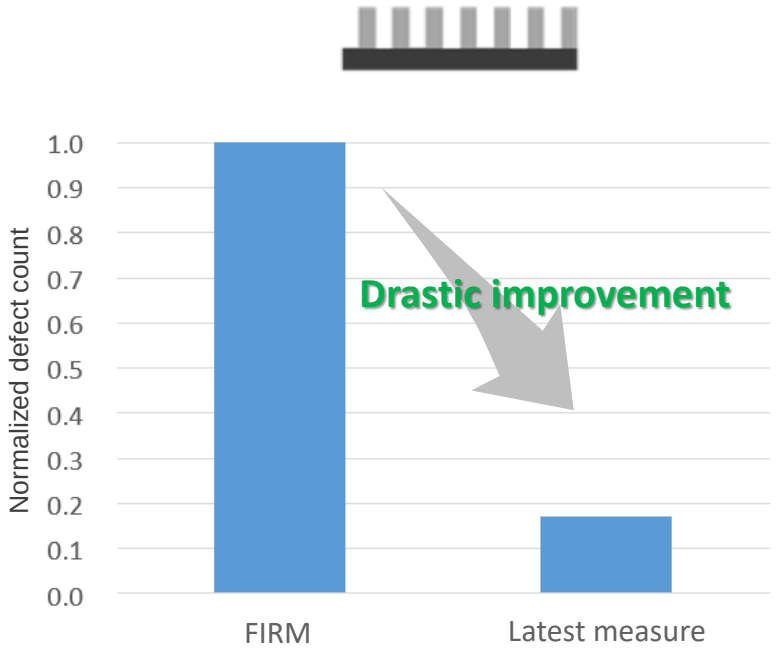
Wider process margin is obtained by latest measure. And pattern height is comparable with existing FIRM process.
→ Latest measure has a potential which can use more higher aspect ratio of EUV PR pattern.

Pattern collapse mitigation effect

- **Post develop**



- **Post etch**



By applying latest measure to the current process, defect level is drastically improved due to pattern collapse mitigation.

Short summary

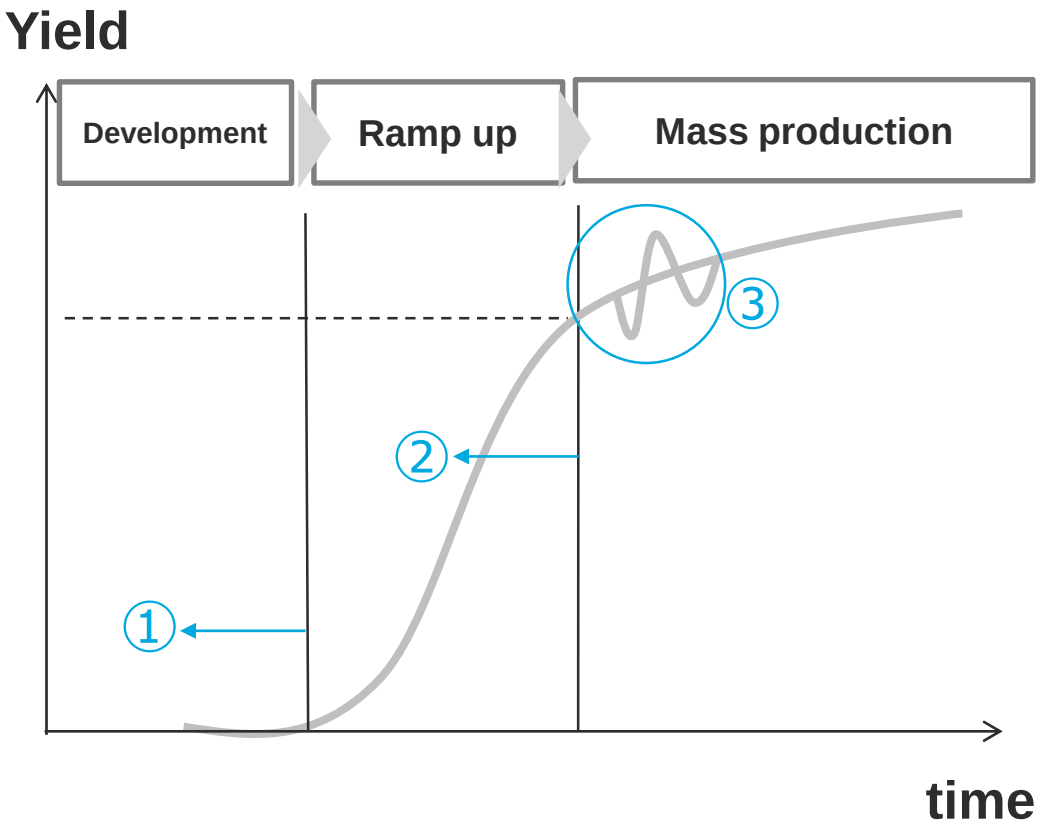
TEL optimized coater and developer process.

1. CH Defectivity performance was improved by in-film particle reduction.
2. LS Defectivity margin was extended by pattern collapse reduction.
3. CD uniformity was improved by development process optimization.

TEL continue to improve EUV process for further EUV high-volume manufacturing.

Coater/Developer system future demand

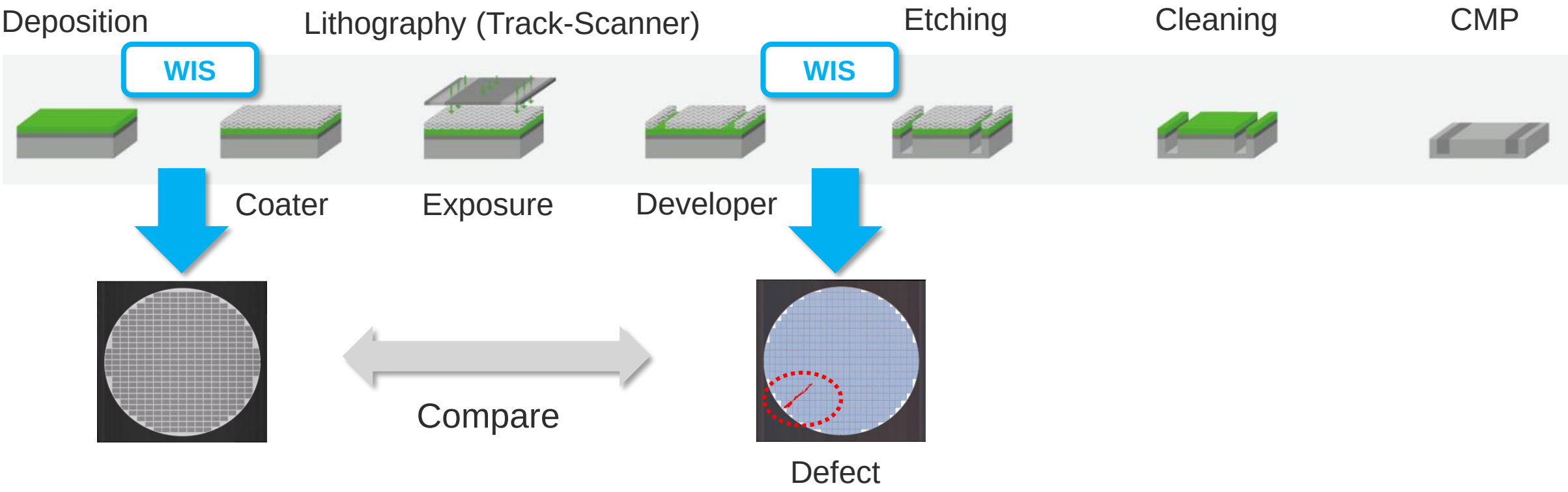
Data use case in semiconductor manufacturing



	Challenge	Data use case example
①	**Development time reduction**	Process simulation
②	**Ramp up time reduction**	Module and tool matching, automation.
③	**Achieve high Yield and good productivity**	Smart sampling, monitor, analysis, diagnostic, prediction, correction.
④	**Automation, Autonomous control which support rapidly expanding Semiconductor manufacturing.**	

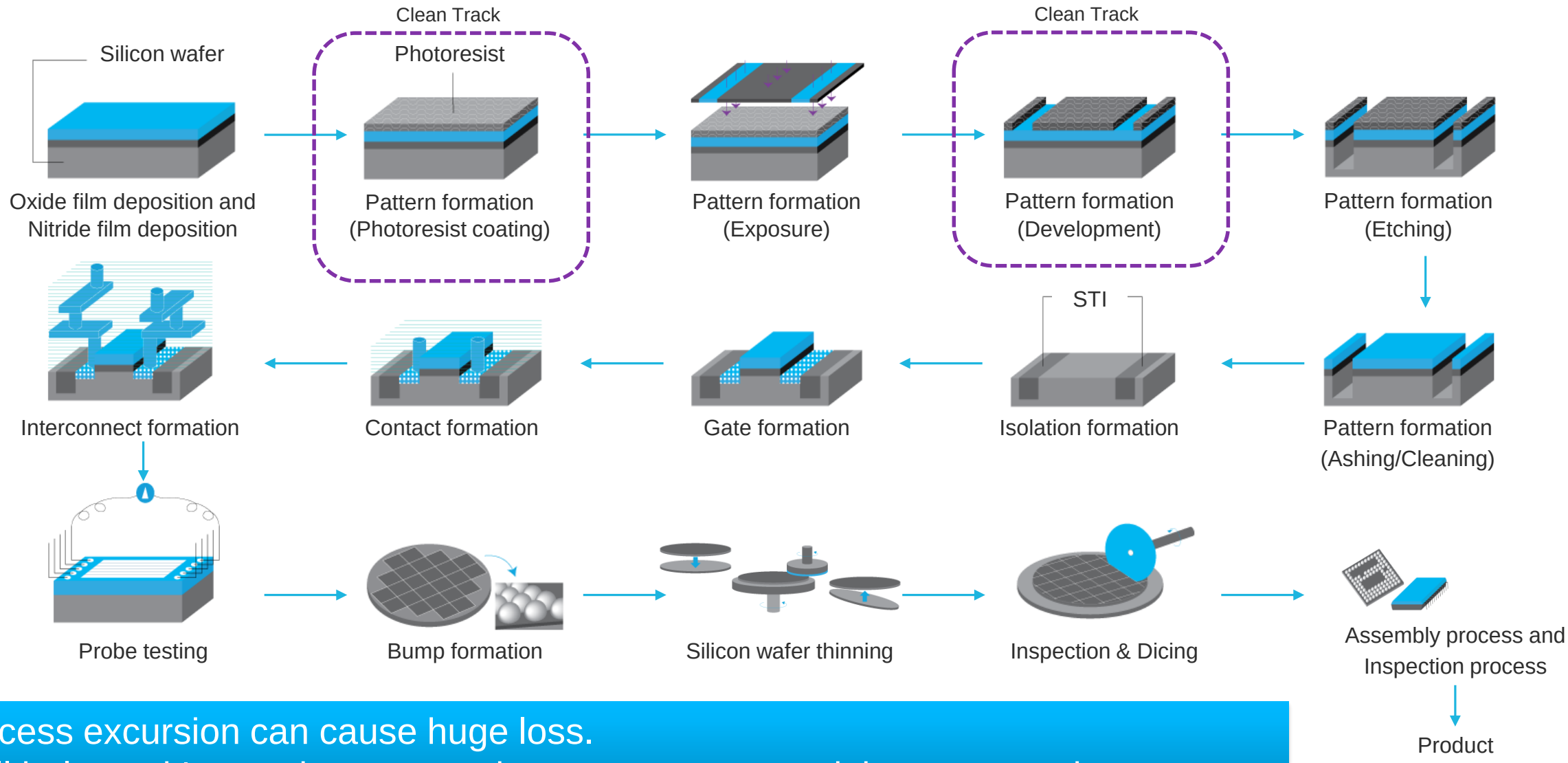
Data generation and usage is key for semiconductor manufacturing

Rapid detection with integrated wafer inspection



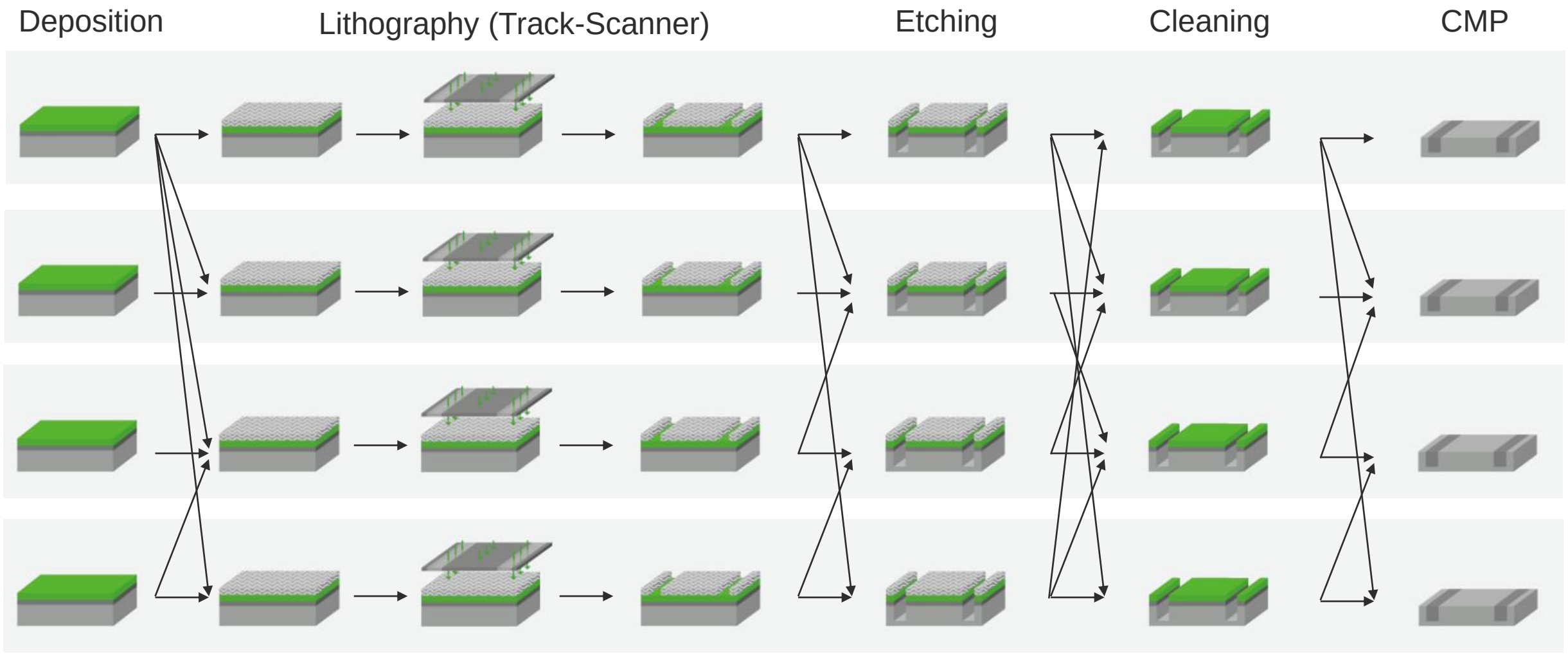
WIS: Wafer Intelligent Scanner

Semiconductor manufacturing process steps are huge

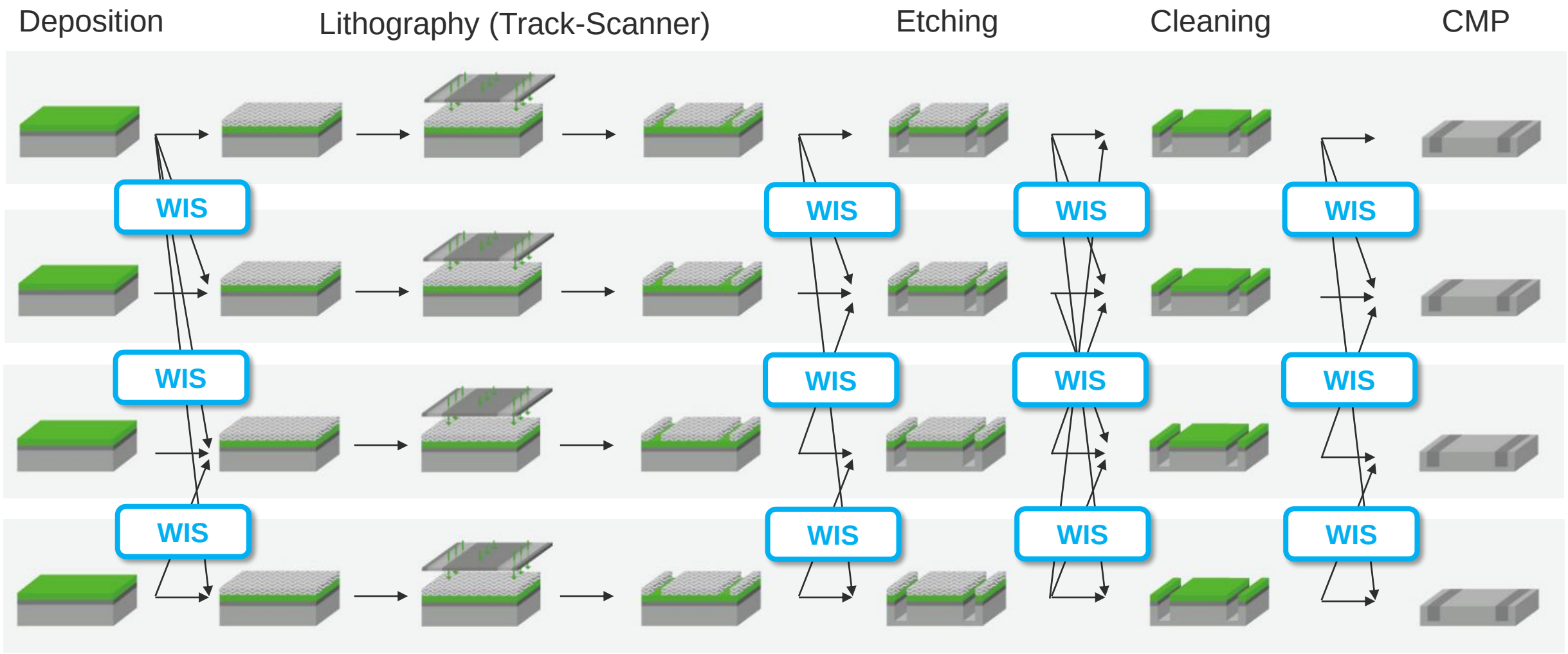


Process excursion can cause huge loss.
Well balanced Inspection cost, no impact to turn around time are very important.

Semiconductor manufacturing wafer paths are so complecated



Inspection everywhere



Macro inspection system with 100% sampling of production wafers

Fast, High and Stable

Customer timeline

Development	Ramp up	HVM (high volume manufacturing)

Availability, Performance, Quality

Matching Analysis

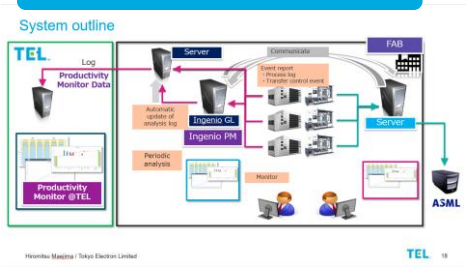
higher

keep

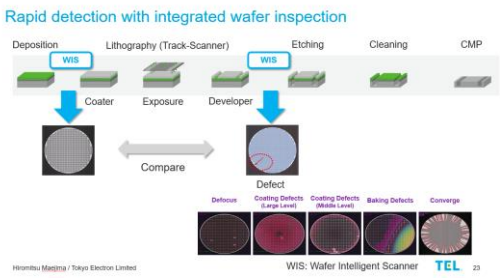
faster

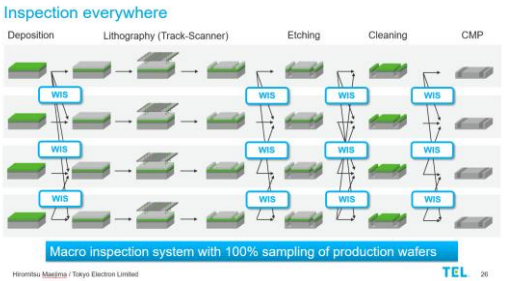
quick recovery

TELeMetrics



WIS





Summary

Summary

- **EUV patterning challenges and TEL's solutions** were reviewed.
- **CLEAN TRACK™ LITHIUS Pro™ Z** reduces in-film particle, pattern collapse and pattern defect with **newly introduced technologies**.

- Future demand of coater/developer system is **Data generation and usage to minimize the Turn around time (TAT) and process excursion**.
- TEL offers valuable contents by using **combined Sensor, Tool knowledge, Data analysis technology.**

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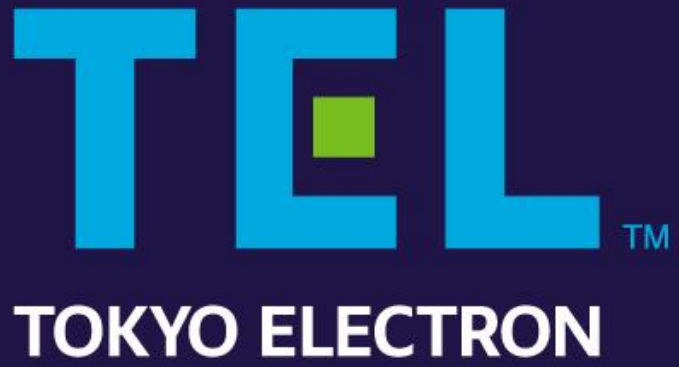
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