Public

OPC Roadmap: Performance Driven Innovation

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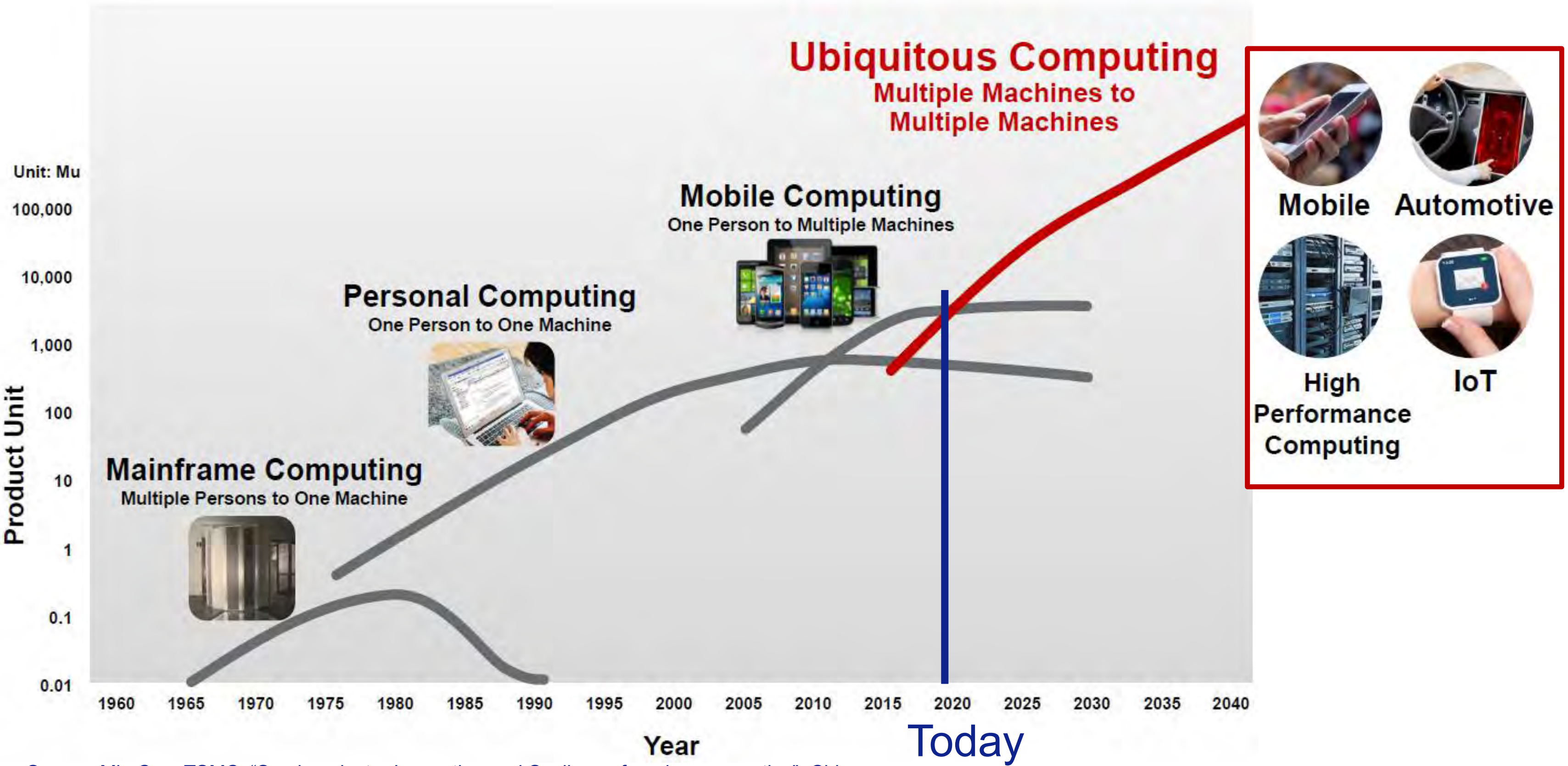
IWAPS October 17-18 2019

Outline

- Roadmap
- EPE Budget
- OPC Model Accuracy
- EPE Metrology and Control
- Summary and Conclusions

Transitioning from Mobile to Ubiquitous computing

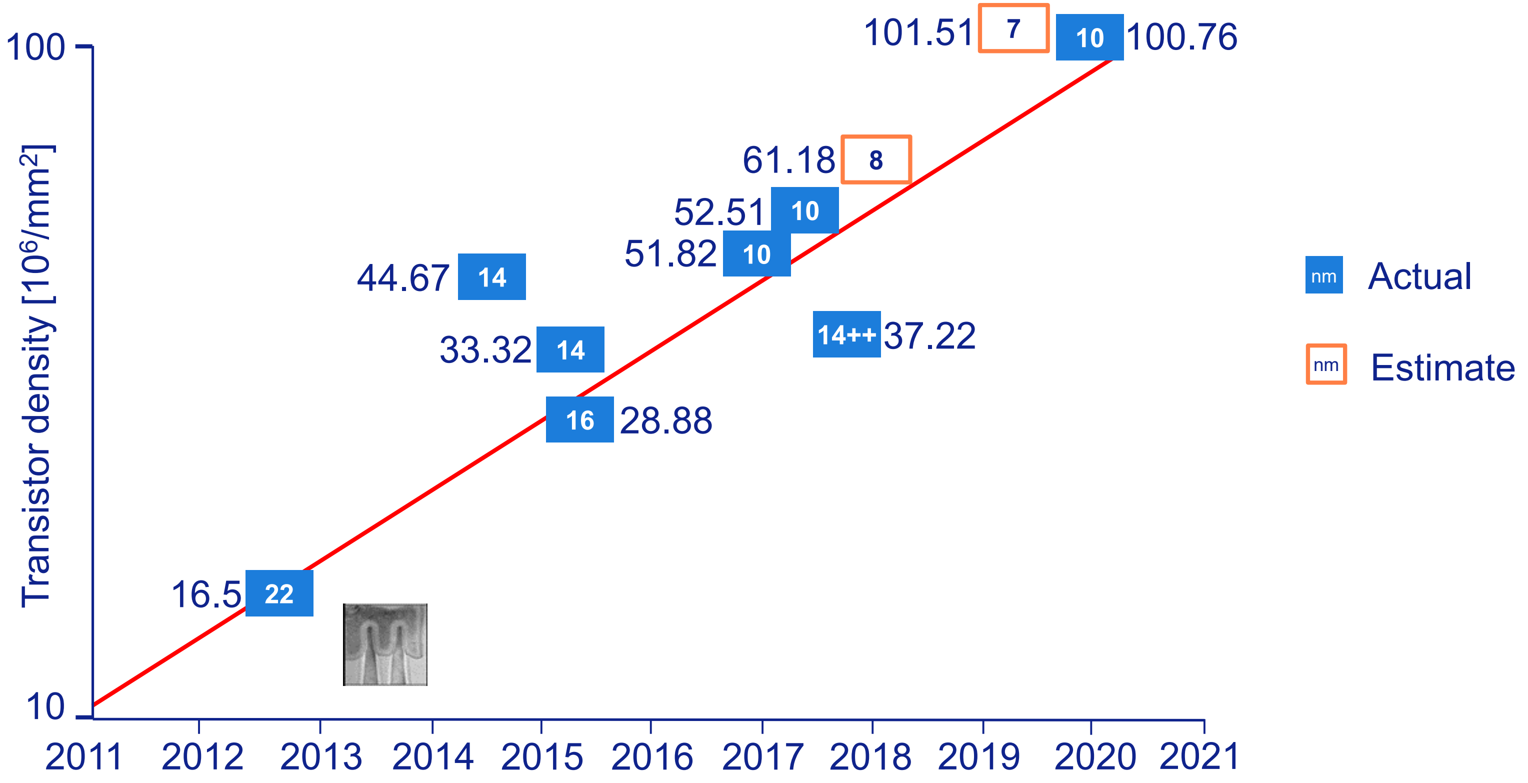
Driven by an unlimited data expansion generated by > 100B products



Source: Min Cao, TSMC, “Semiconductor Innovation and Scaling, a foundry perspective”, China Semiconductor Technology Conference, Shanghai, March 2019

Transistor density increase is still at 2x per 2 years

Moore's Law continues….



Source: Mustafa Badaroglu, International Roadmap for Devices & Systems' 'More Moore' briefing (November 2018)

Logic roadmap: 2D scaling for >10 years, evolving to 3D

Innovation in devices continues …

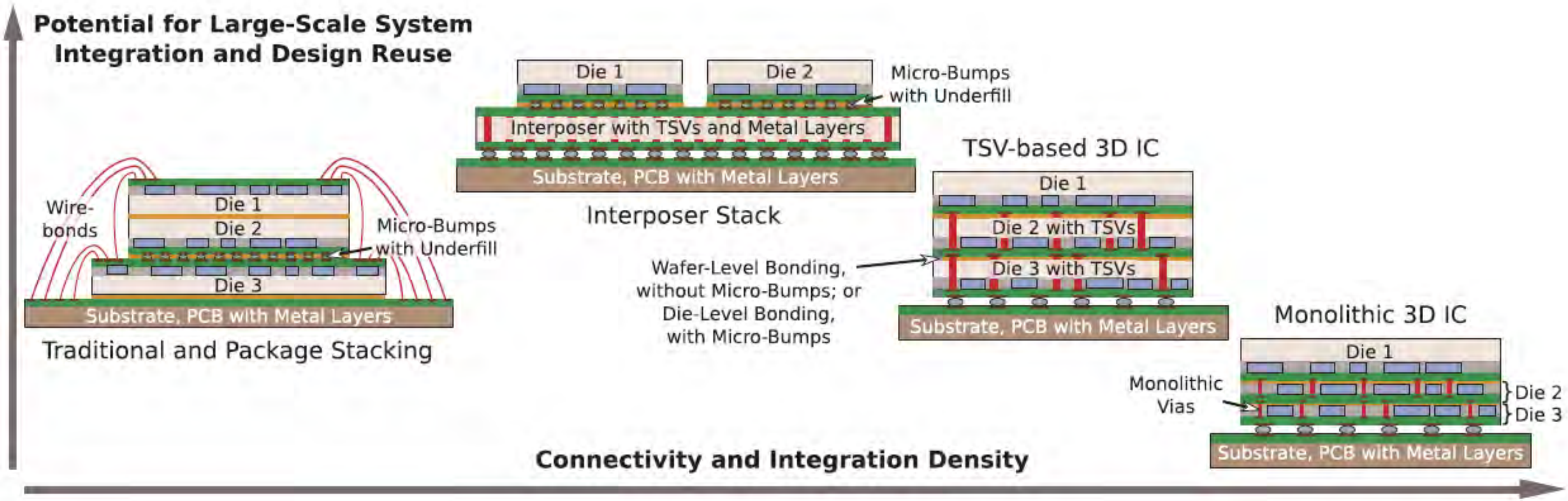
Year of production	2018	2020	2022	2025	2028	2031	2034
Poly/Metal Pitch (nm)	P54M36	P48M32	P45M24	P42M21	P36M16	P36M12	P36M12
Logic 'node range' labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.5"	"1.5"
Logic device structure options	FinFET FDSOI	FinFET	FinFET LGAA	LGAA VGAA	LGAA VGAA	LGAA VGAA	3DVLSI VGAA
Logic mainstream device	FinFET	FinFET	FinFET	LGAA	LGAA	VGAA	3DVLSI

Trend confirmed by multiple logic customers ⟵ | ⟶ Speculative

Source: Mustafa Badaroglu, International Roadmap for Devices & Systems' 'More Moore' briefing (November 2018)

Plenty of innovation in system/chip integration

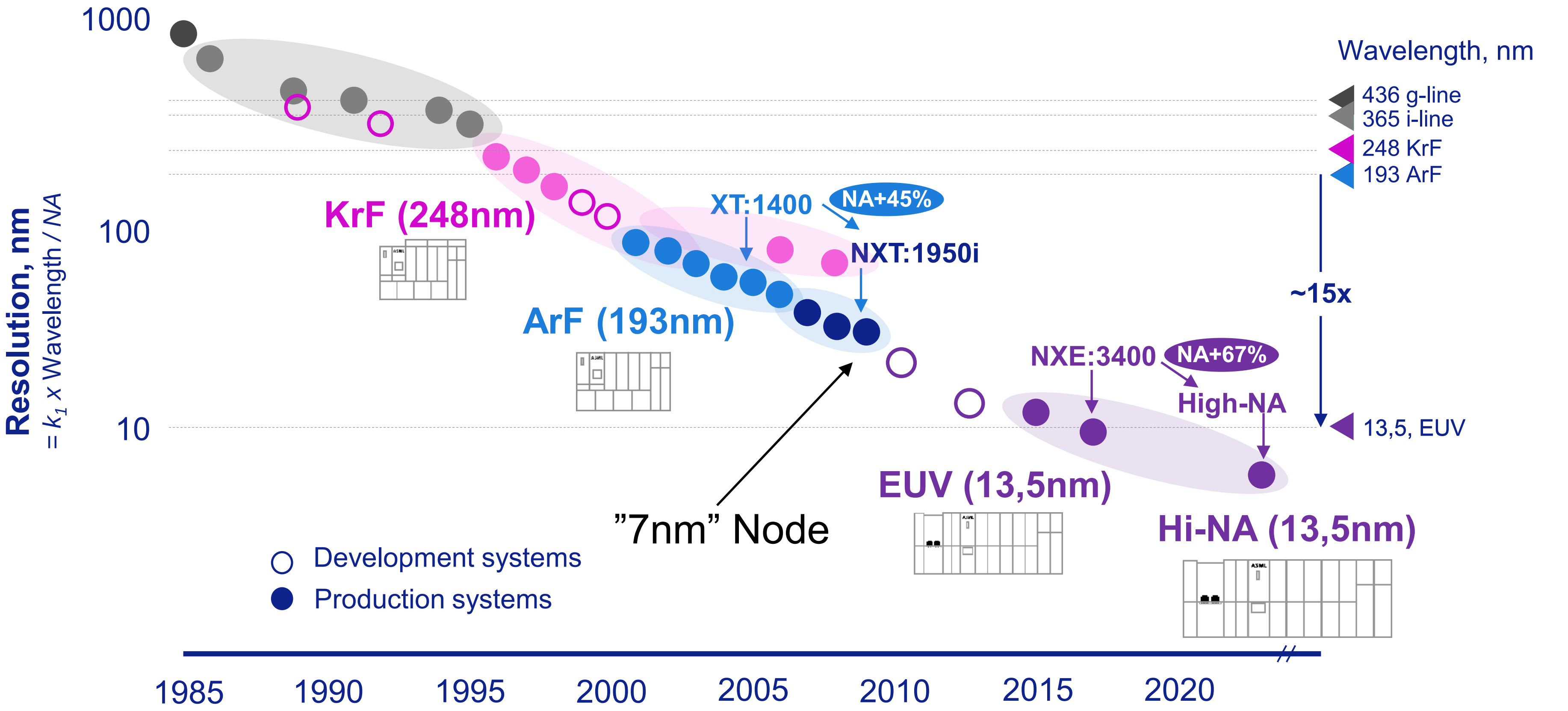
Exciting possibilities to improve system performance



J Knetchel et al, IPSJ Trans System LSI Design Methodology Vol.10 45–62 (2017)

EUV Era Extends Lithography Roadmap

Resolution Limit < 10 nm



J van Schoot et al, Proc. SPIE Vol. 11147 (2019)

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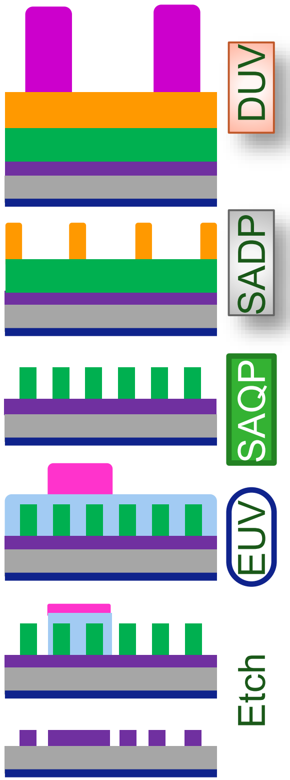
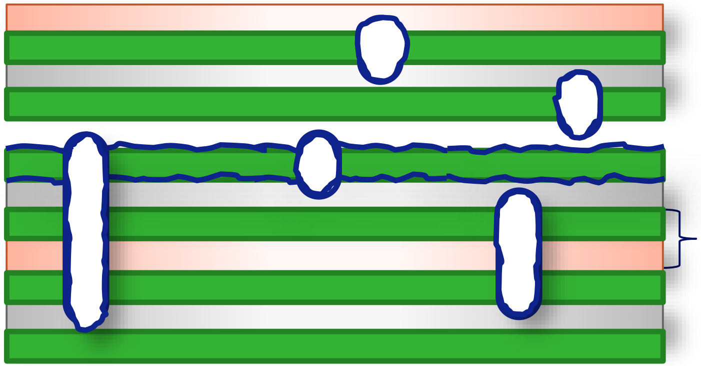
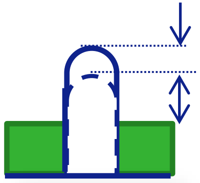
Patterning minimum pitch is limited by EPE variation

EPE is extreme value of all overlay (OL) and CD errors combined







EPE is the relative displacement of the edges of two features from their "target position

Local errors (LWR, Line Width Roughness)

Pitch (P)

Max EPE ≈ P/4

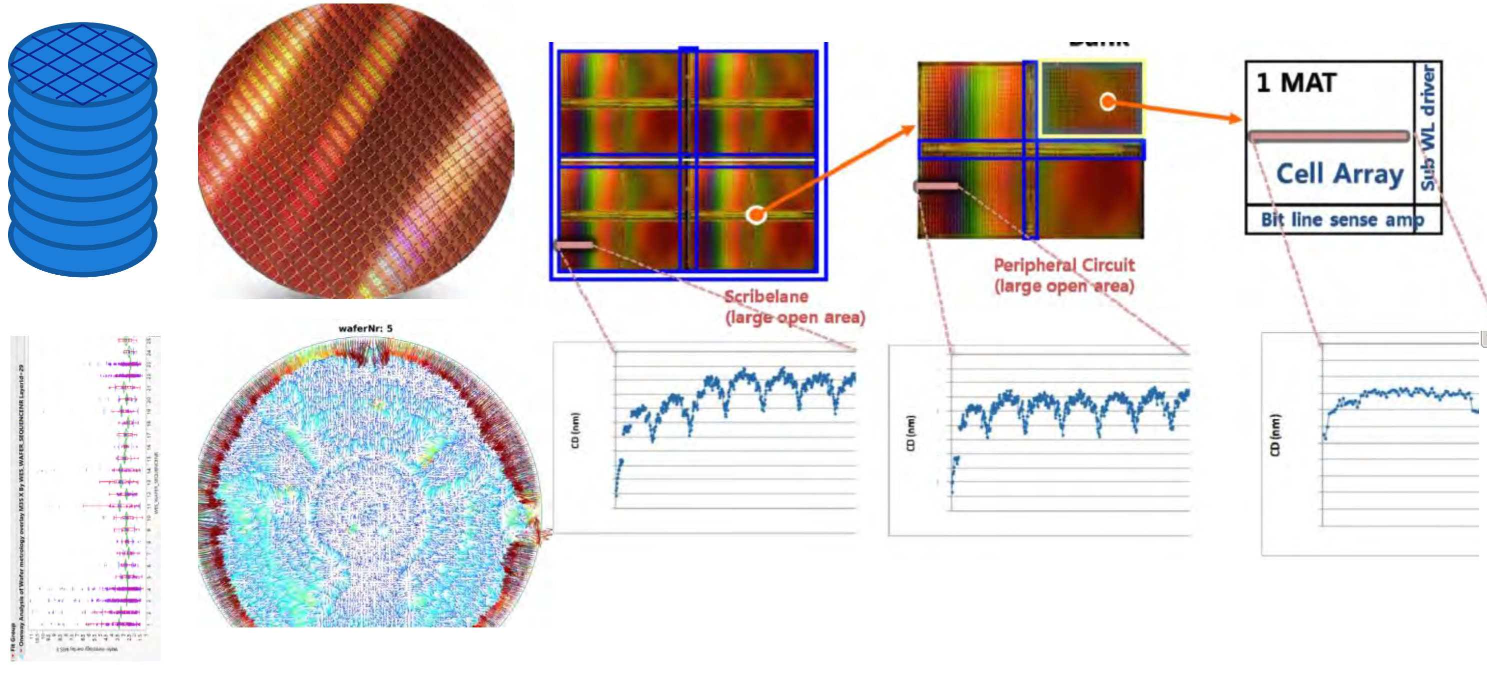
$$EPE = \mu_{EPE} + 3\sigma_{EPE} = \frac{HR_{OPC}}{2} + \frac{3\sigma_{PBA}}{2} + \frac{6\sigma_{LWR}}{\sqrt{2}} + \sqrt{(3\sigma_{overlay})^2 + (\frac{3\sigma_{CDU}}{2})^2}$$

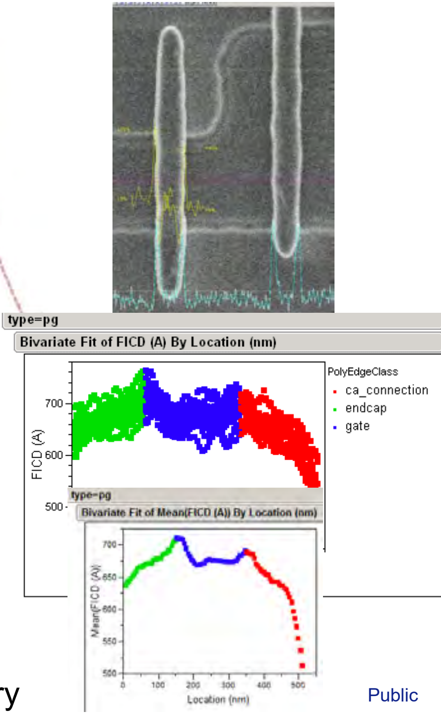
* Model presented by Richard Schenker at SPIE 2016

EPE Variation length scales span >30cm to <1um

CD and Overlay fingerprints exist across all length scales

Lot (>30cm) | Wafer (30cm) | Field (3cm) | Die (8mm) | Memory Array (80um) | Device (<1um)

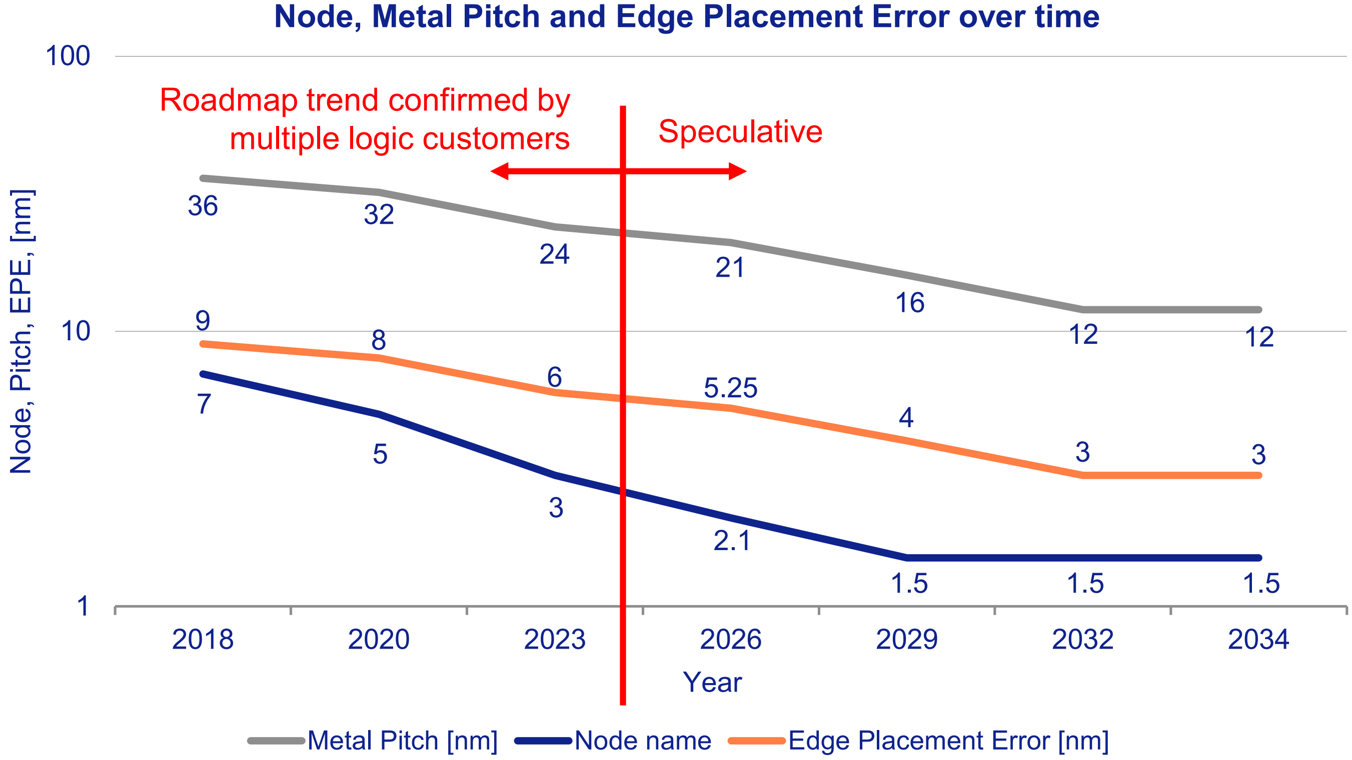




Wafer Figure from K. Kim SPIE 2016; Overall figure from Cyrus Tabery

Looking ahead: Edge Placement towards 2035

The next 10 years is about 2D scaling, then evolving to 3D scaling



CC Wei (CEO) in Q1 2019 TSMC Earnings Call, Murthy Renduchintala (Chief Engineering Officer) in Intel Investor Conference in May 2019

Source: Mustafa Badaroglu, IDRS More Moore out brief, Nov 2018, (International Roadmap for Devices and Systems)

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OPC

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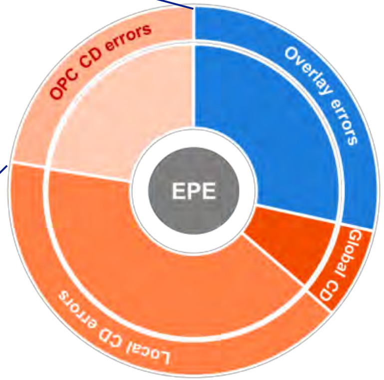
EUV **CD & EPE** (2-D) ADI OPC Error Budget

OPC ~ 25% of EPE Budget → 2 nm 3σ CD target

Class	OPC & Reticle Item	EUV 1.5D/2D Budget Contribution
OPC	algorithm convergence	**minor**
ADI Model	Model form	**significant***
	AI model accuracy	**significant***
	Mask-Manufacturing Model Residual (MPC)	**significant***
	Metrology Accuracy Model Residual	**significant***
	Measurement Uncertainty	**significant***
	Simulation Grid Dependency	**minor**
	Through Slit Corrections	**significant***



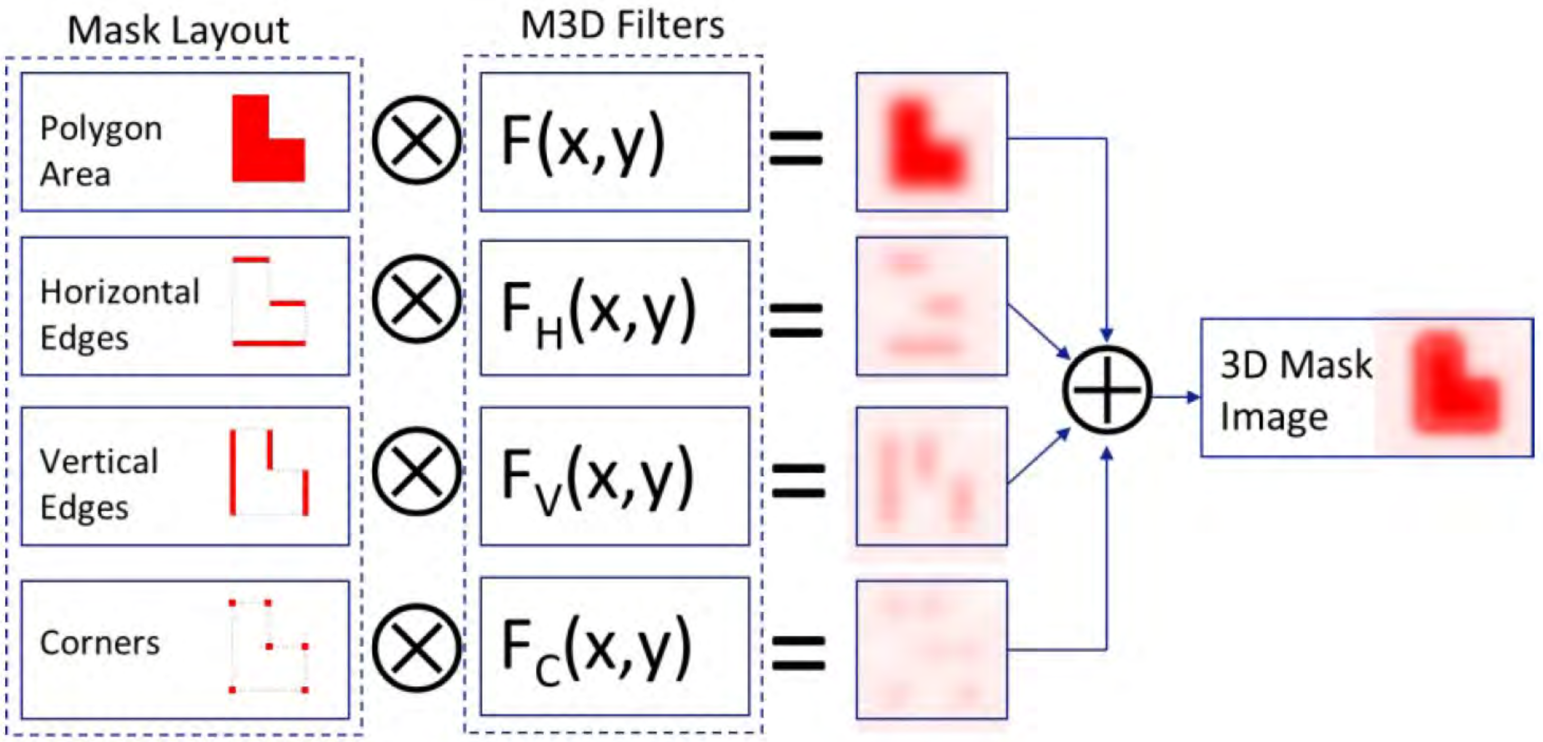
- This presentation focuses we will show how driving improvements in all these areas drives OPC improvement

* > 1.0 nm 3σ

Modeling

Aerial Image is starting point for OPC

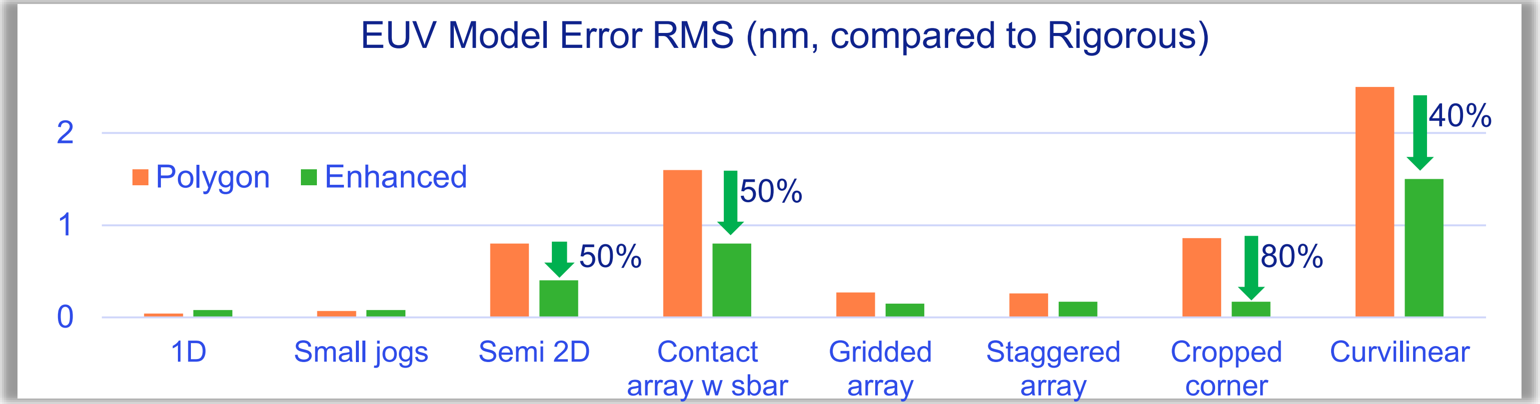
Clever Approximations Enable Fast Accurate Simulation

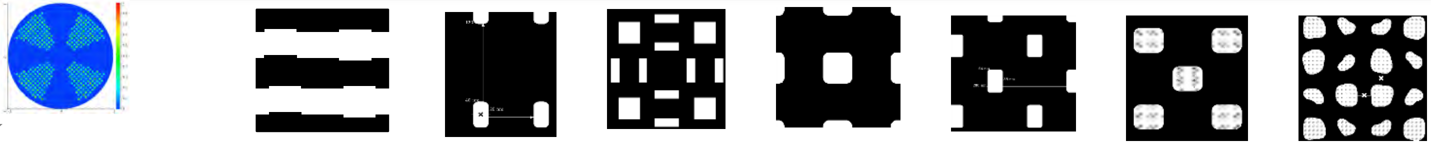


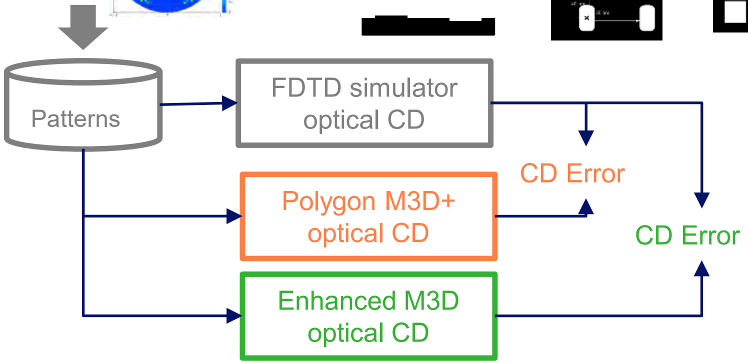
P. Liu et al, Proc. SPIE Vol. 8676 (2013)

Aggressive RET on EUV Masks Increases Challenge

Continuous Innovation Required





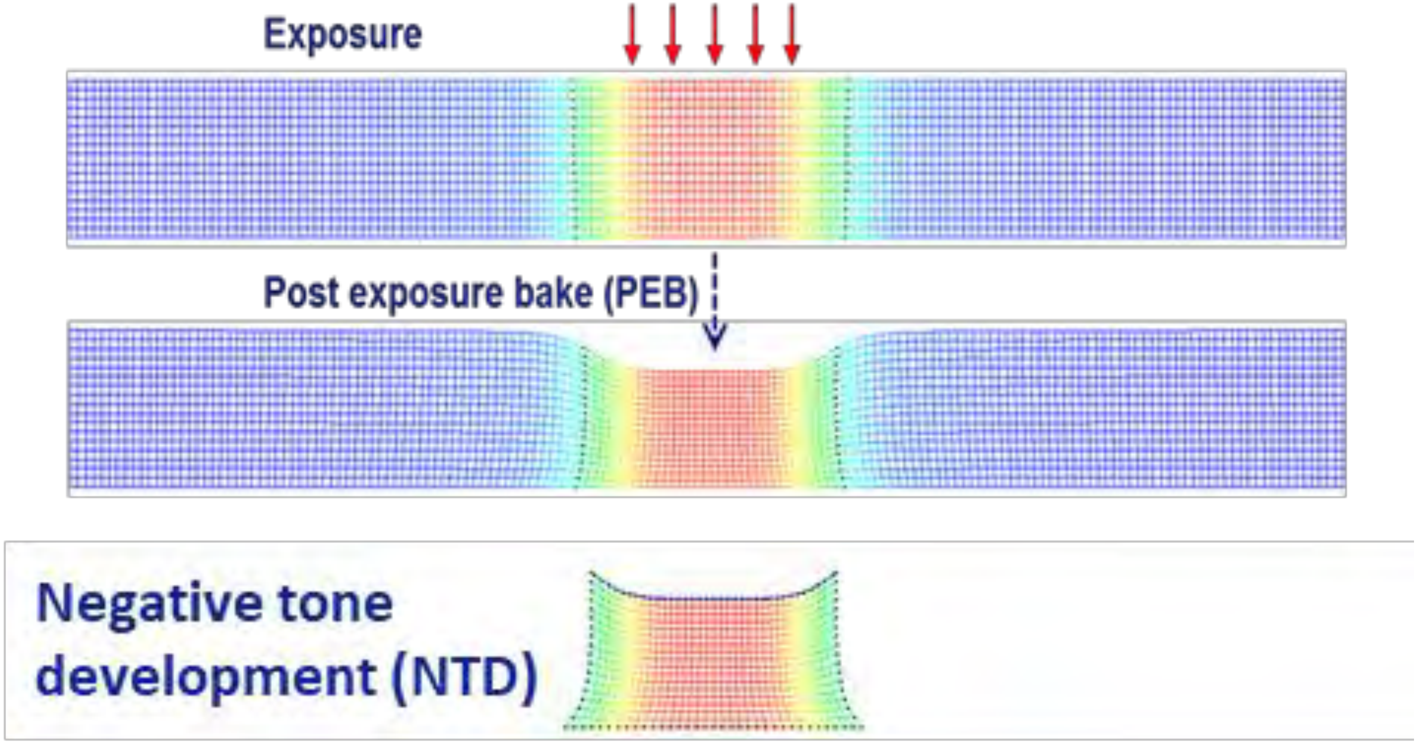


Selected EUV patterns with

- 1D
- Small jogs
- Semi 2D
- Contact array with sbar
- Gridded array
- Staggered array
- Cropped corner
- Curvilinear

Physical Model Development Still Important

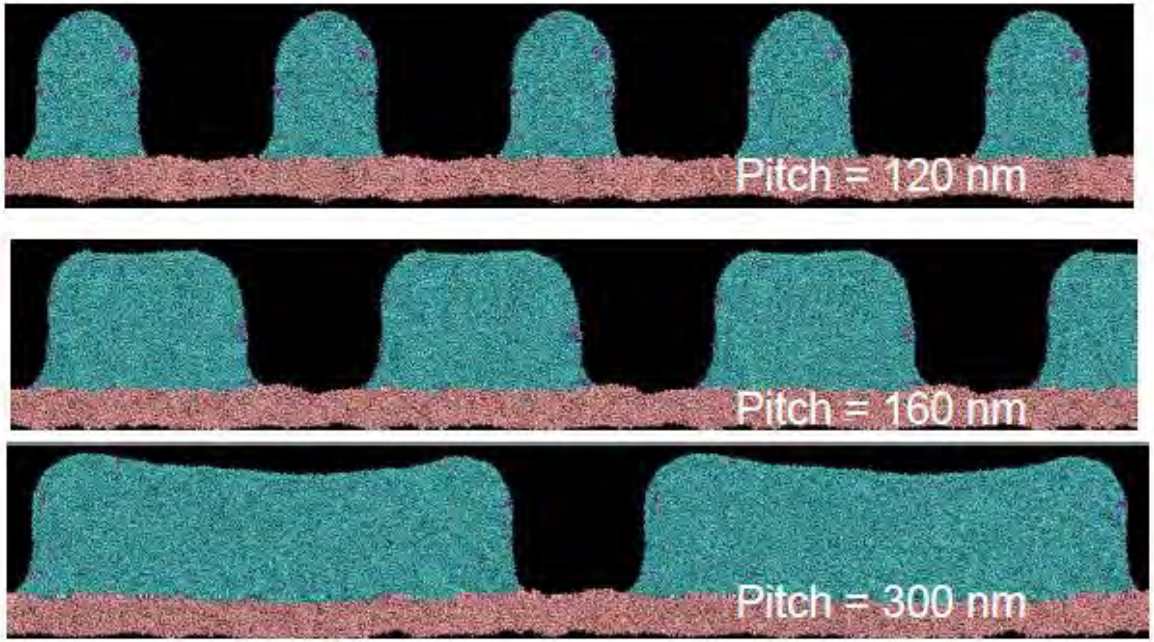
Finite Element Models help understand Physical Shrink in NTD resists



P Liu et al., Proc SPIE Vol. 9779 (2016)

Molecular Modeling for Molecular Control

Molecular Dynamics provides insights for compact models



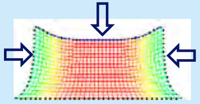
C Batistakis et al, Intnl Conf of Photopolymer Science and Technology (2016)

Deep Learning Is Next Step

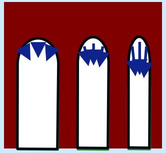
Enabled by fast e-beam metrology and physical based models

Stability

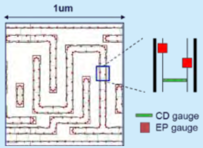
Physical driven **training** using physics based lithography models



Physical Resist Shrinkage



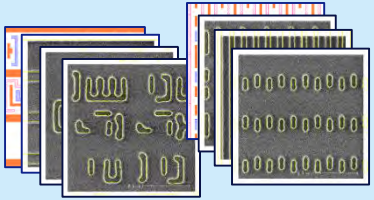
Resist surface stress



Data expansion through simulated contours

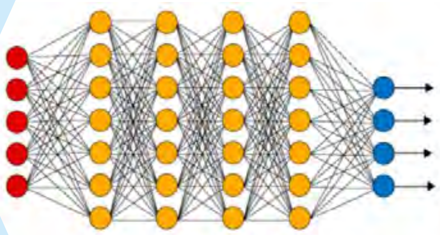
Accuracy

Data-driven **training** based on fitting spec and wafer measurements

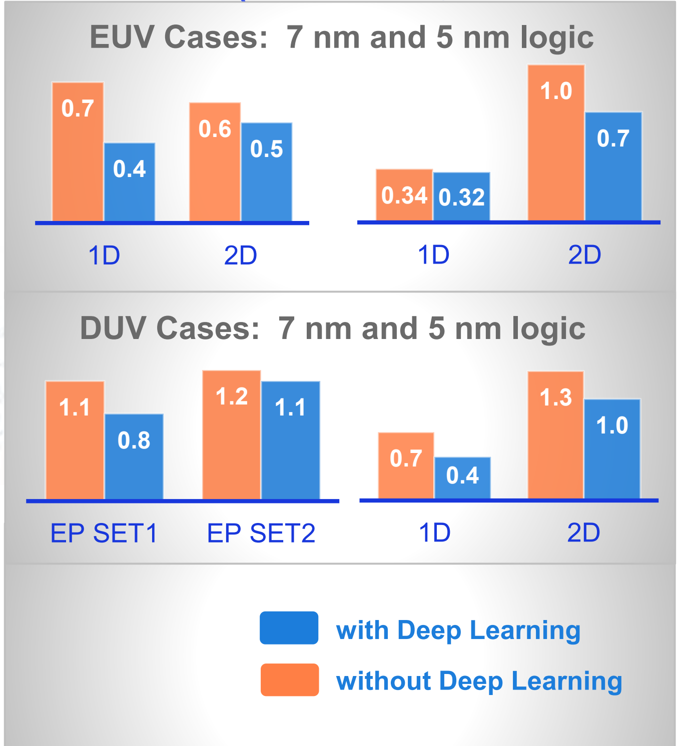


Large volume wafer metrology data, further enhanced by fast e-beam

ASML Deep Learning model



Model Prediction Accuracy (RMS in nm)



"EP SET1" → Edge Placement Gauge Set 1

Deep Learning for Etch Modeling

Tachyon Effective Etch Bias (EEB) models

$$bias = \sum_i c_i Term\_bias_i + const\_bias$$

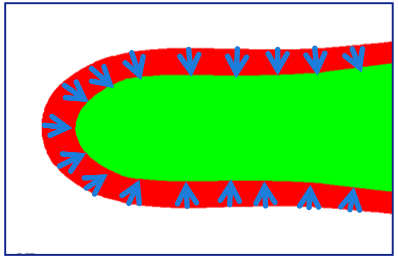
Real etch process

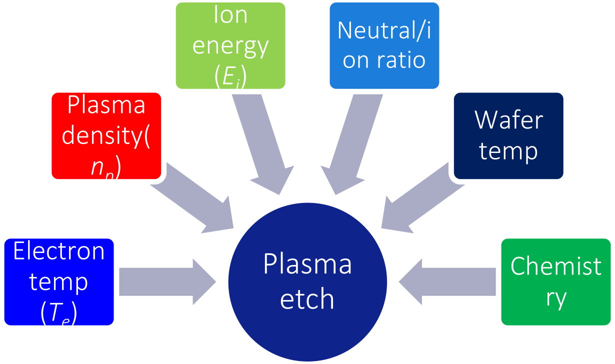
- Etching and passivation mechanisms coupled together
- Complicated etch behavior

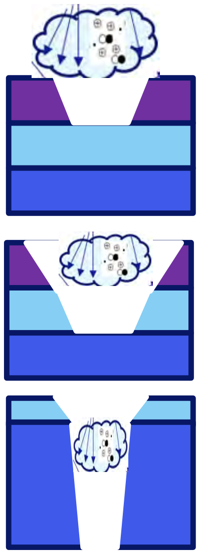
Deep learning

- Capture unknown & complicated etch physics
- Learn from wafer contour

Term based EEB model



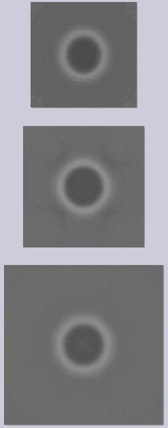
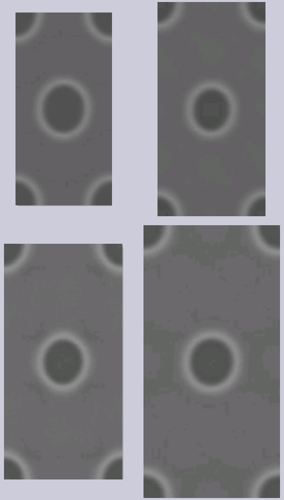
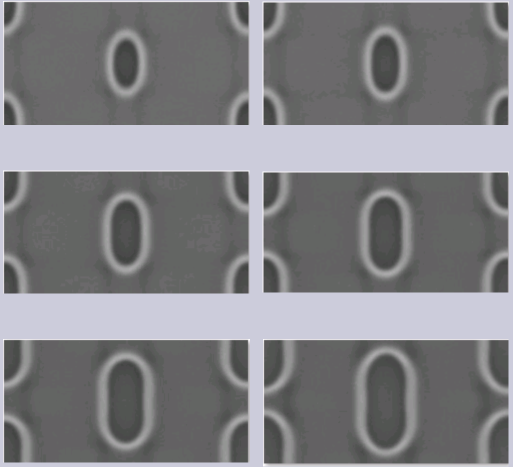
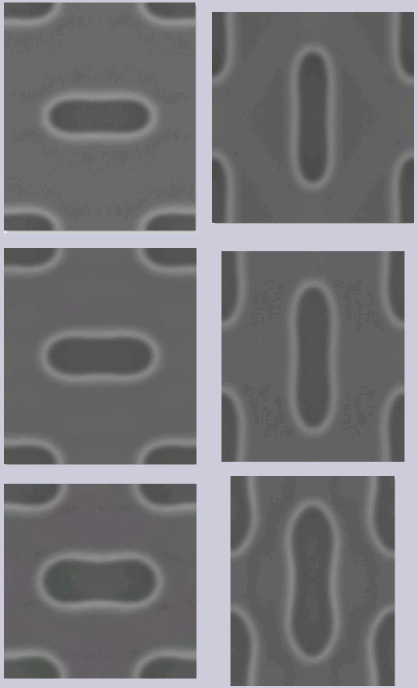




SEM Metrology

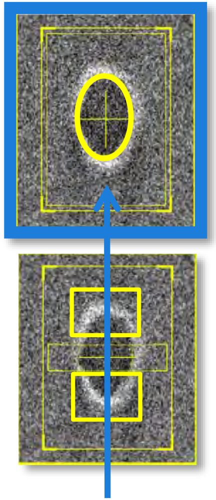
OPC Metrology has Large Diversity

Challenge to derive ACCURATE measurements for all gauges

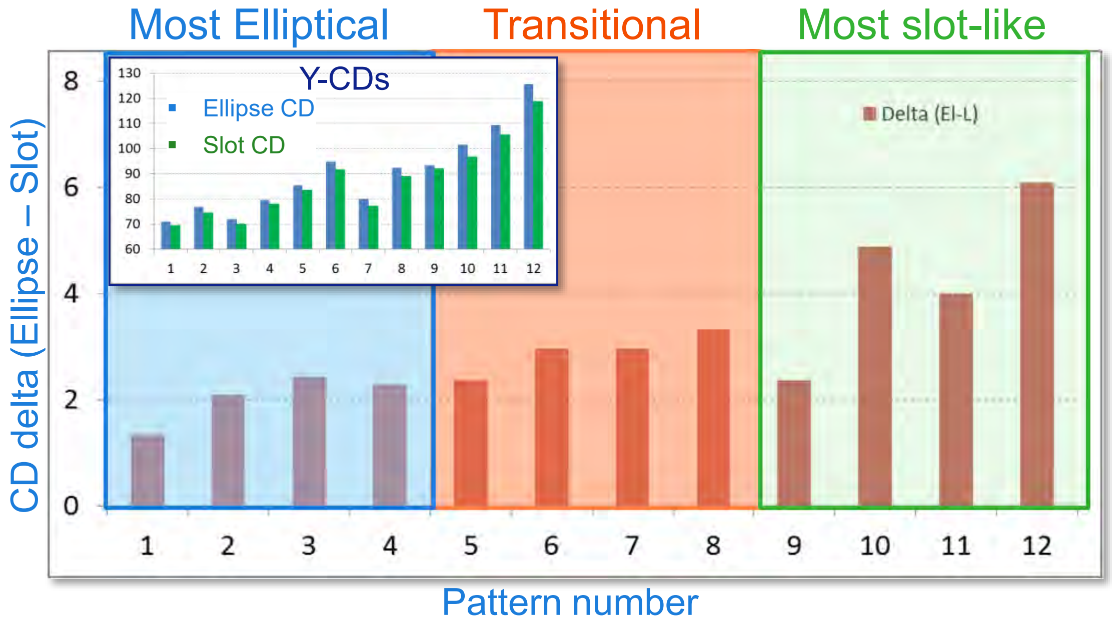
Orthogonal cuts AR = 1	Staggered cuts AR = 1	Orthogonal cuts AR ~ 2	Staggered cuts AR ~ 2	Staggered cuts AR >3
				

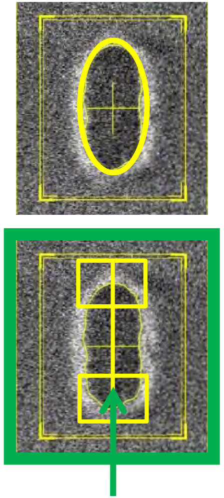
T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

An example of shape-fit algorithm differences: long axis ellipse-to-slot transition



Best algorithm for 'most elliptical' shapes





Best algorithm for 'most slot-like' shapes

Mean shape-fit shift: 3.4 nm (in transitional region)

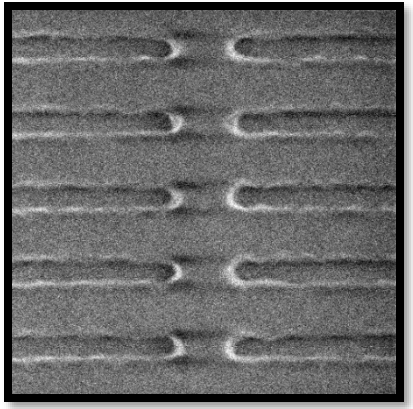
Range of shape-fit shift: 3.6 nm (transitional region inter-pattern bias range)

Shape fits can create algorithm-based CD offsets between very similar features

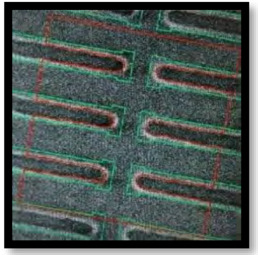
T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

Resist charging disproportionately affects 2D measurements and algorithms

e-beam scan direction



Charging bands distort contours and measurements



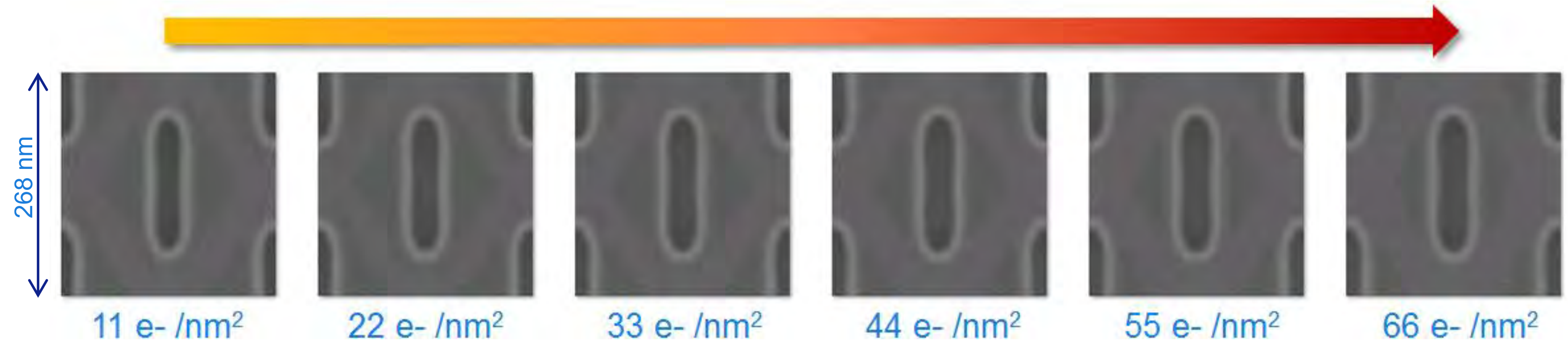
Charging bands can be partially mitigated by scan rotation

Charging is due to basic physics of e-beam:resist interaction

Charging distortions are dynamic and depend on interaction of SEM scan and pattern shape

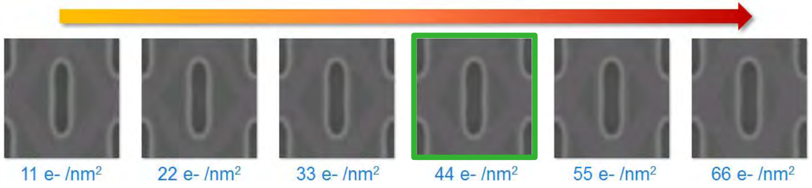
T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

2D SEM damage evolution

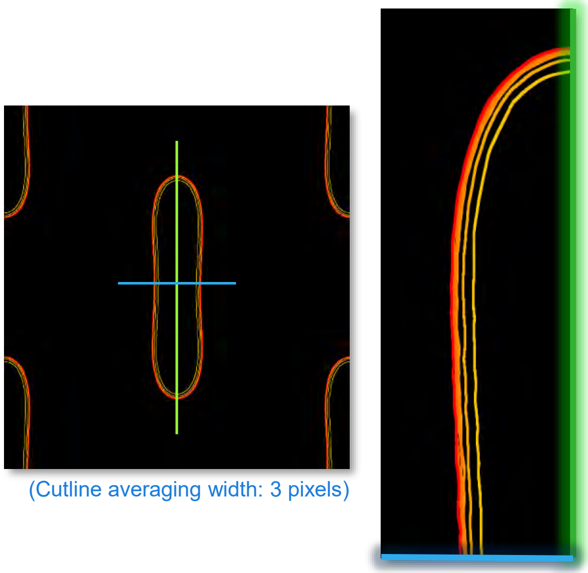


T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

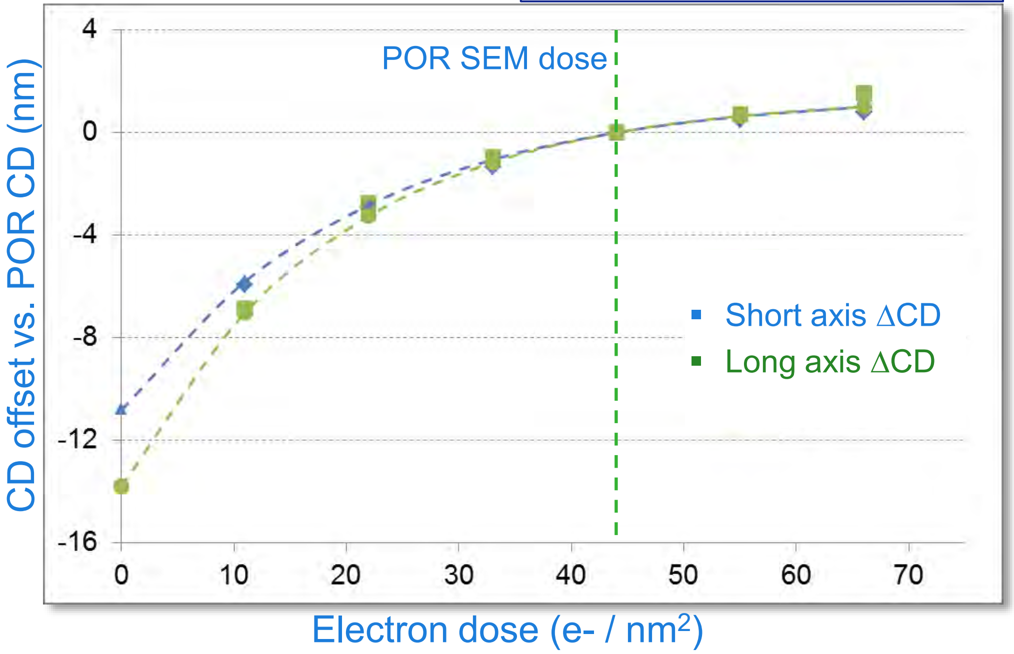
Aspect ratio bias becomes larger as damage increases



$$CD_{(n)} = CD_{(o)} + A \cdot \exp(-\gamma \cdot n) - A$$



(Cutline averaging width: 3 pixels)



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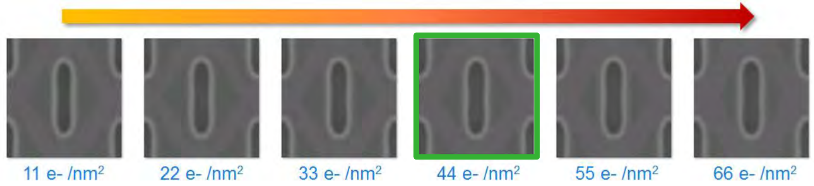

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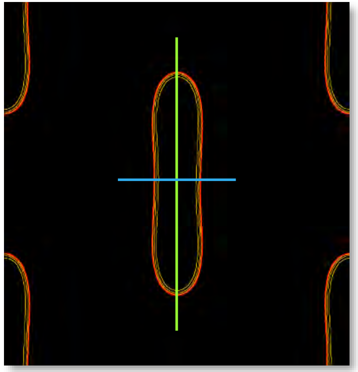

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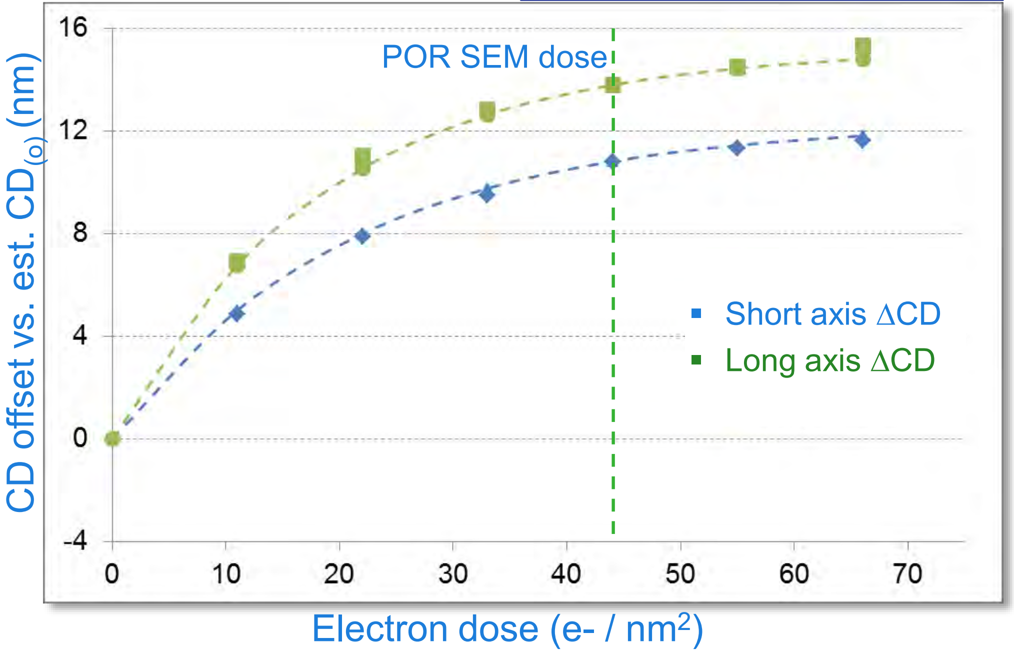


T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

SEM Metrology Distorts Patterns

Errors are significant part of overall OPC Model Error Budget

Key summary: model accuracy and metrology

ASML

Model accuracy roadmap

	2016	2017	2018	2019
1D Model calibration error range	3~4 nm	2 nm	1.6 nm	1.4 nm
2D Model calibration error range	6 nm	5 nm	4 nm	3 nm

OPC metrology challenges

	SEM damage		Charging	Measurement Practice		
	(high vs. low dose)	(zero damage estimate)	Scan rotation	Threshold (est. 10% range)	Image filtering (est. 1.5σ range)	Shape-fit methods
Mean CD difference	6.4	11.8	2.4	1.7	1.4	3.4
Inter-pattern bias range	2.5	6.1	4.3	1.4	2.1	3.6

Different measurement methods can:

- change measured CDs by up to 15 nm
- change inter-pattern biases by up to 6 nm

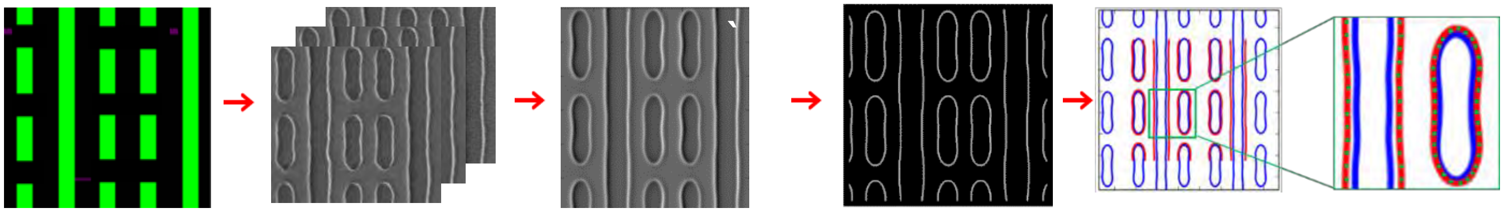
T. Wallow et al., Proc. SPIE Vol. 10145 (2017)

Contour Based metrology Improves Model Accuracy

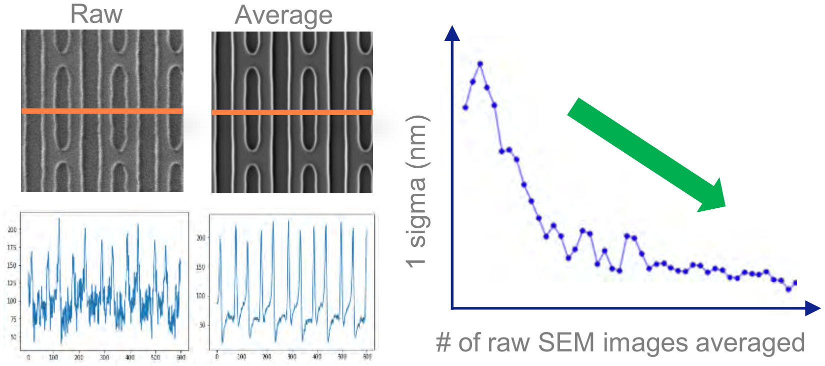
Reduces Random Noise, Shape Fitting and EP Gauges

MXP provides accurate contour metrology for OPC model calibration and verification

Design Pattern → Images → Averaged Image → Precise Contour → Edge Placement (EP) Gauges



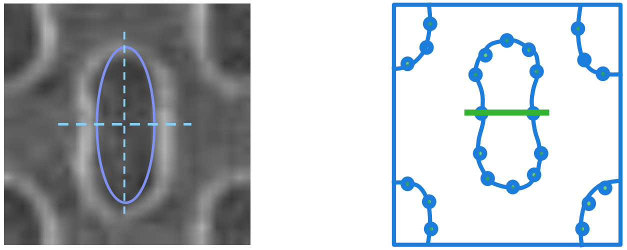
Random noise reduction



Shape fitting improvement

CD-SEM
Systematic fitting error

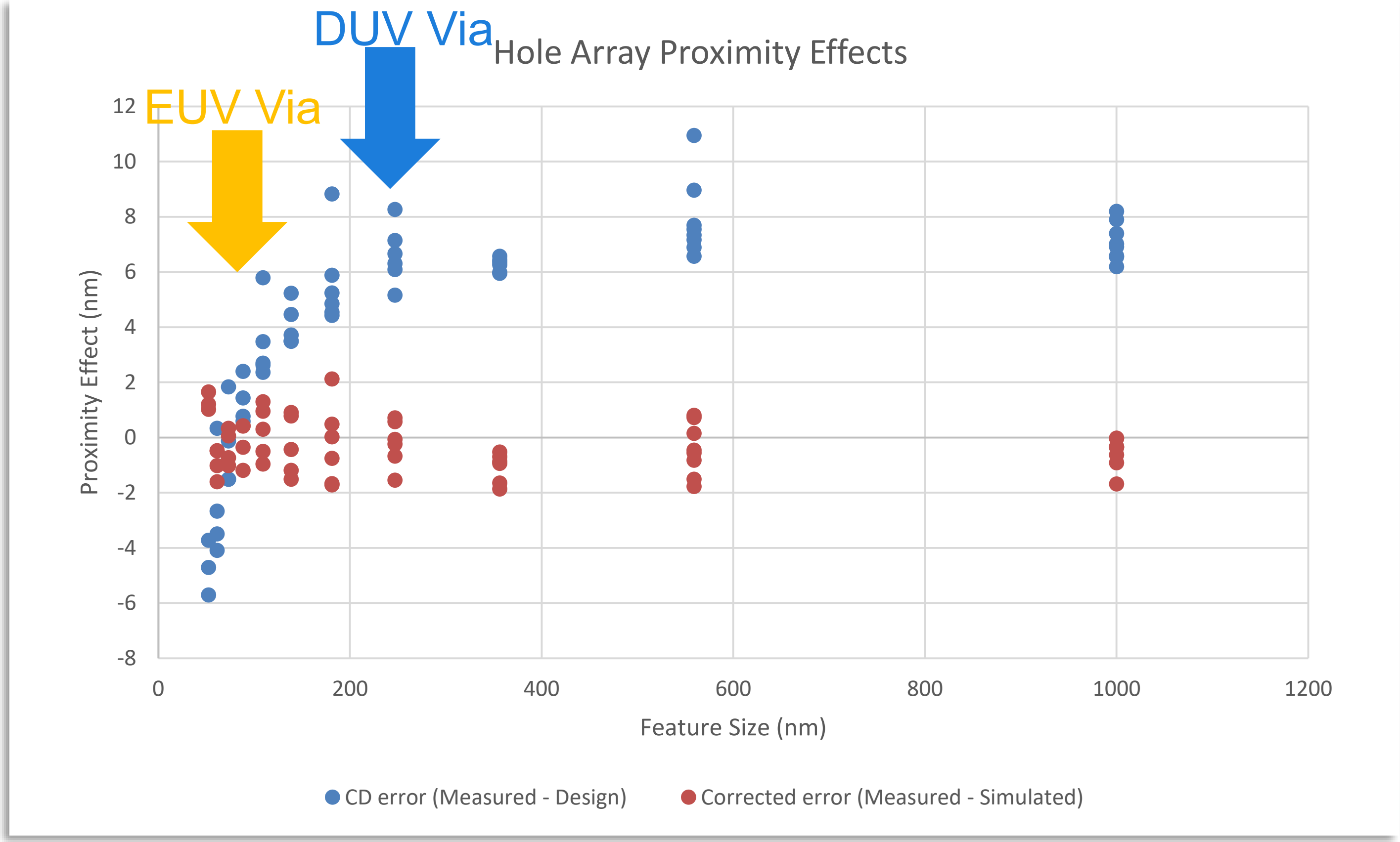
MXP
Direct measurement



Mask

Smaller mask CD for EUV Masks

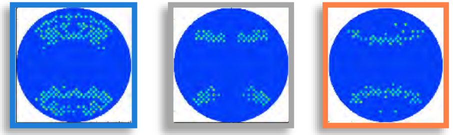
Increases impact of Mask Proximity Effects

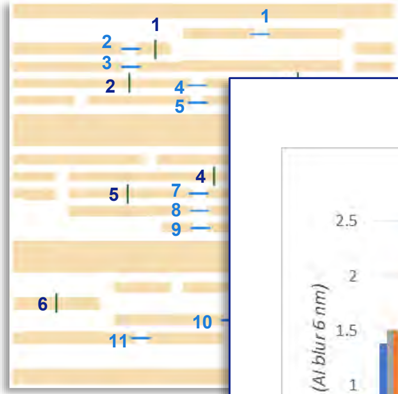


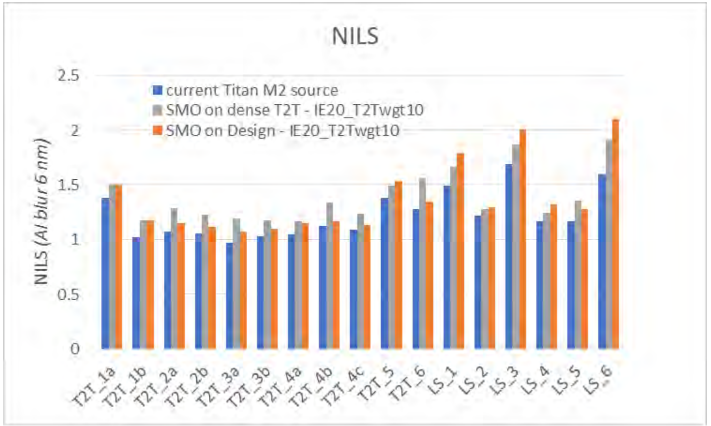
T. Wallow et al, Proc. SPIE Vol. 11147 (2019)

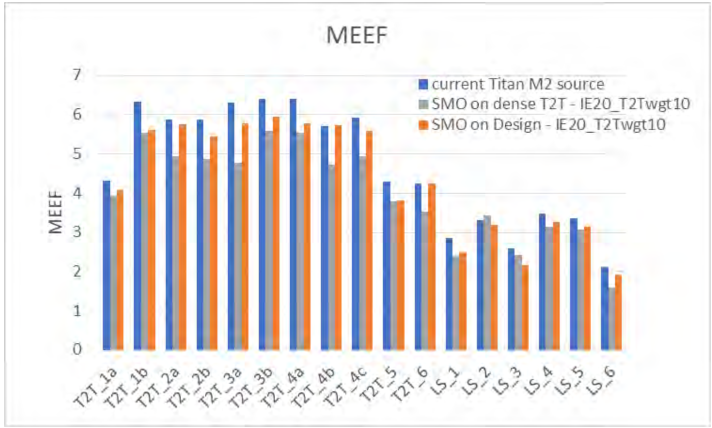
EUV 2D patterning will include patterns with MEEF > 4

Small mask errors may have big impact on wafer









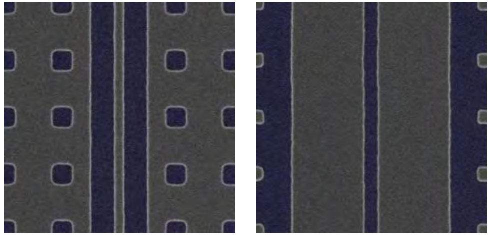
iN5 Metal 32nm Pitch (Rio et al. BACUS 2018)

T. Wallow et al, Proc. SPIE Vol. 11147 (2019)

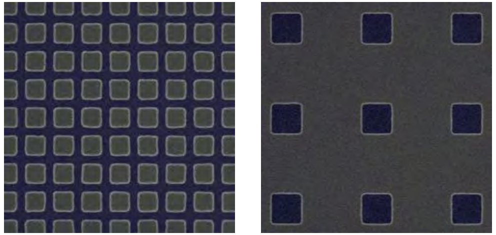
MPC model calibration test case

IMEC ‘Genesis’ EUV reticle

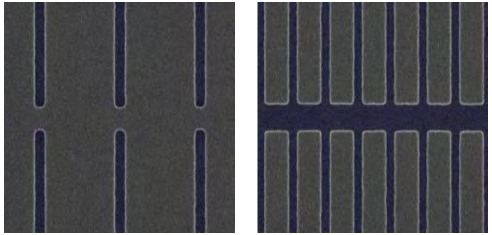
line/space
(8%)



density
(79%)



holes and pillars
(3%)

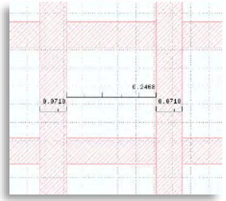


line-end and space-end
(10%)

~4000 patterns; mix of 1D, 1.5D (‘density’) and 2D

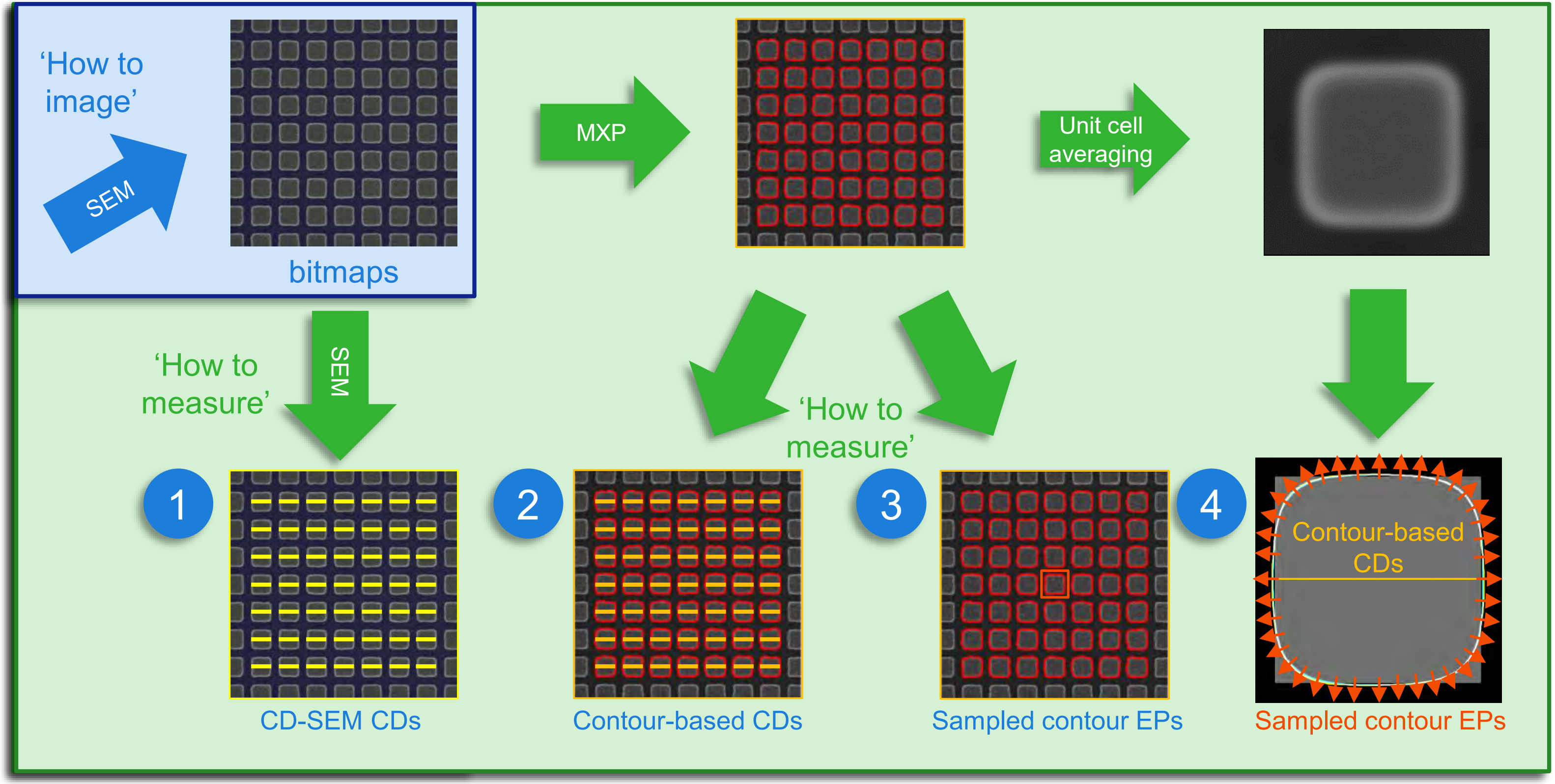
Full image set is measured using different metrology methods

Metrology method overview



Measurement definition

(Design-based metrology)



Each method yields method-specific measurements.

T. Wallow et al, Proc. SPIE Vol. 11147 (2019)

Co-improvement of metrology and MPC model

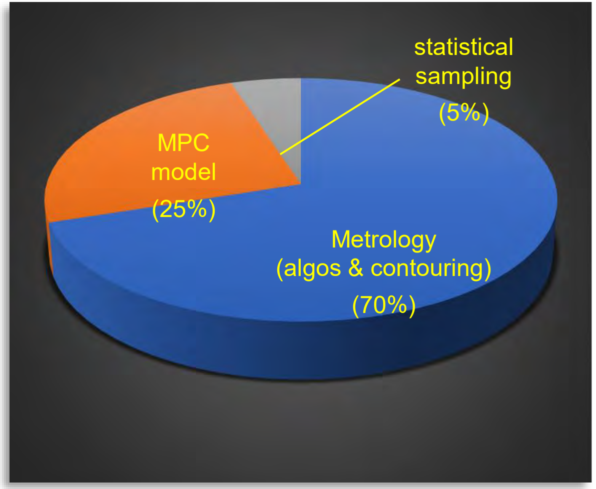
POR MPC calibration

Metric	Value (nm)
rms error	1.43
error range	17.5

Improved MPC calibration

Metric	Value (nm)	Improve-ment (%)
rms error	1.01	29
error range	9.9	43

Co-improvement cycles



~30% overall model accuracy improvement from iterative process

T. Wallow et al, Proc. SPIE Vol. 11147 (2019)

Outline

- Roadmap
- EPE Budget
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- **EPE Metrology and Control**
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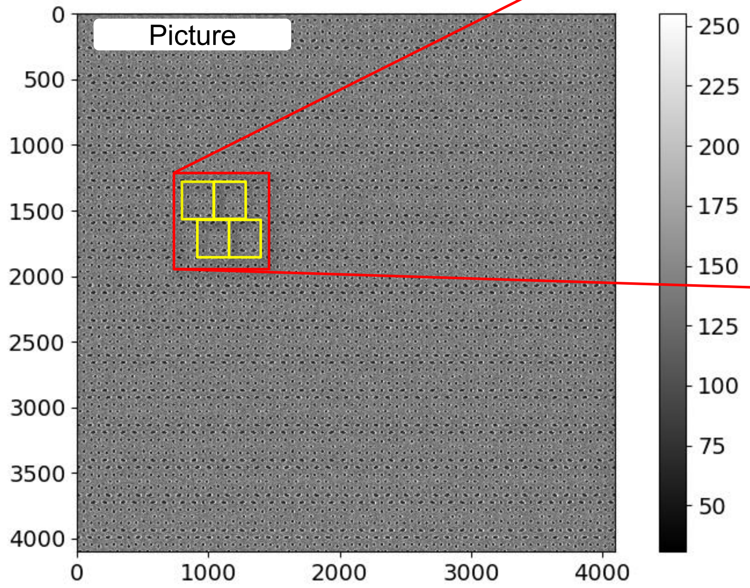
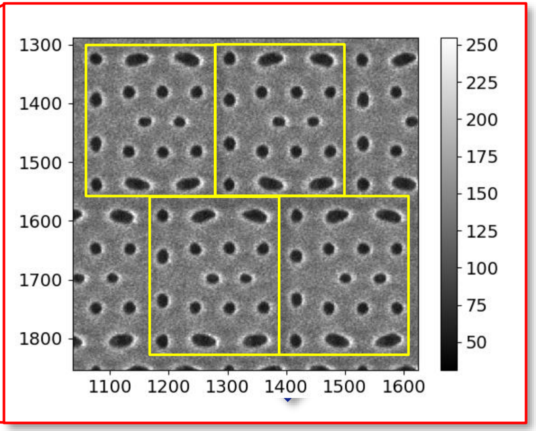
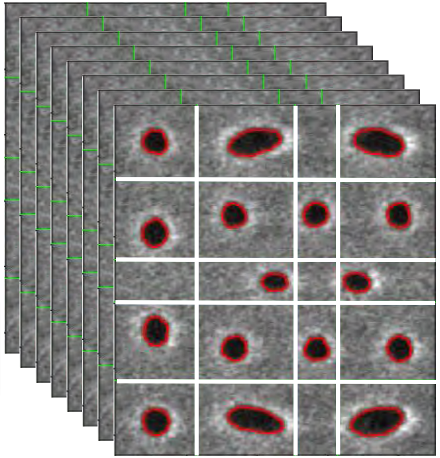
Contour

Each picture contains 238 unit cells

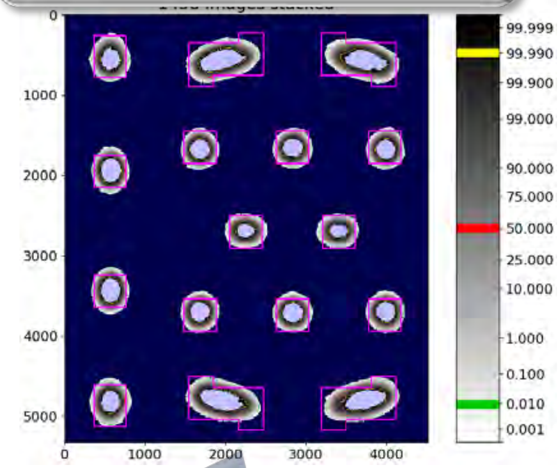




For every unit cell contours are extracted and converted to labeled polygons



1455 images x 238 unit cells contours are stacked (about 350k unit cells)



Contours are aligned and stacked to draw an Edge position probability map

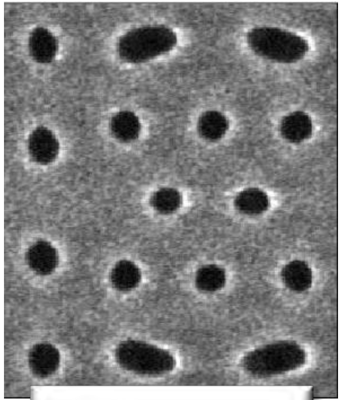
life.augmented

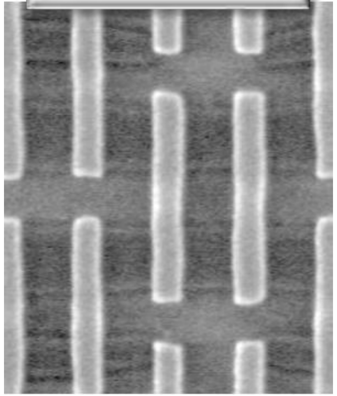
ASML

B Le-Gratiet et al, Proc. SPIE Vol. 10959 (2019)

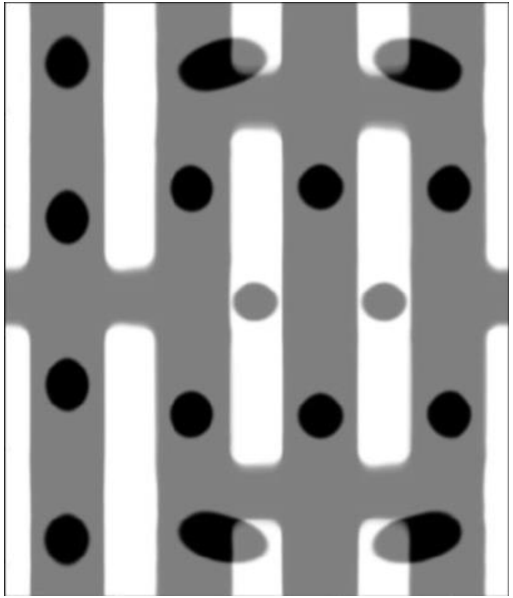
Public

EPE analysis (2 layers)

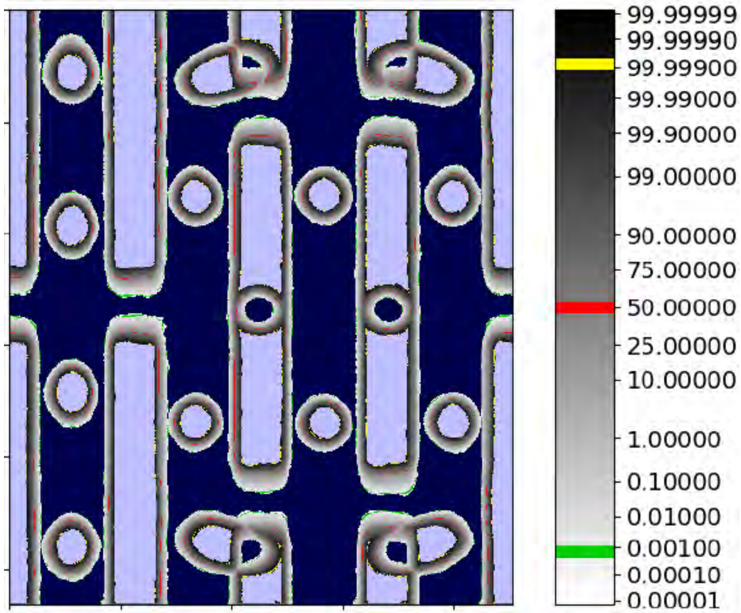




Unit cell images



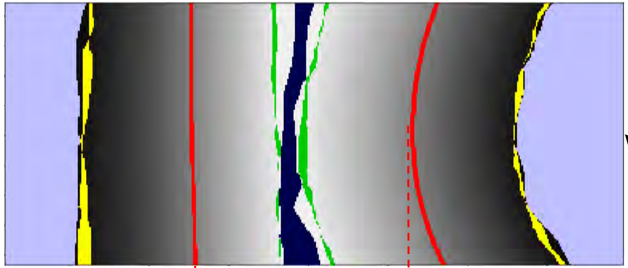
Gray level linear scale stacked map

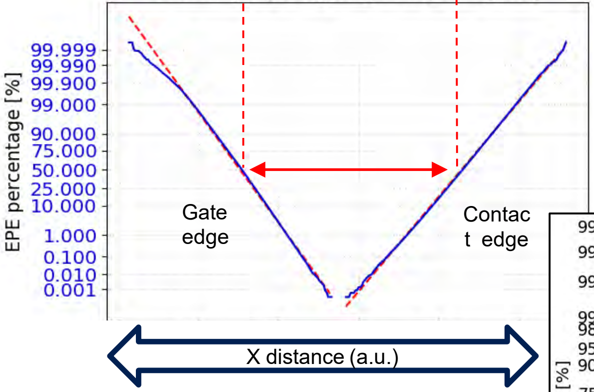


Probability map (of edge)

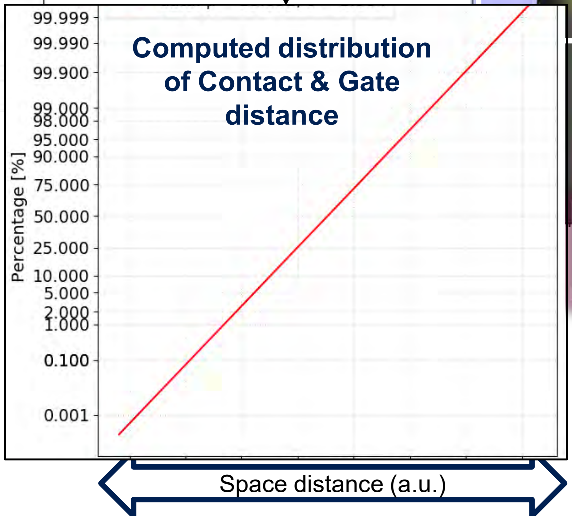
Reminder: Contact profile are taken post Contact Etch (TOP).
In product contact edges are critical at « mid height » post CMP and W-fill ➔ smaller CD's

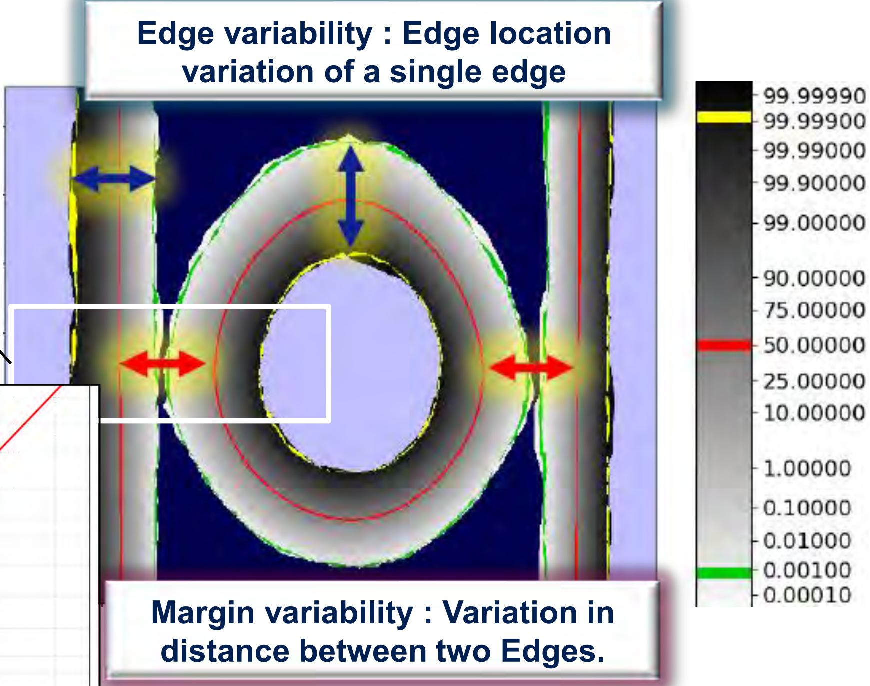
EPE analysis (2 layers)





Position distribution of both Contact & Gate edges

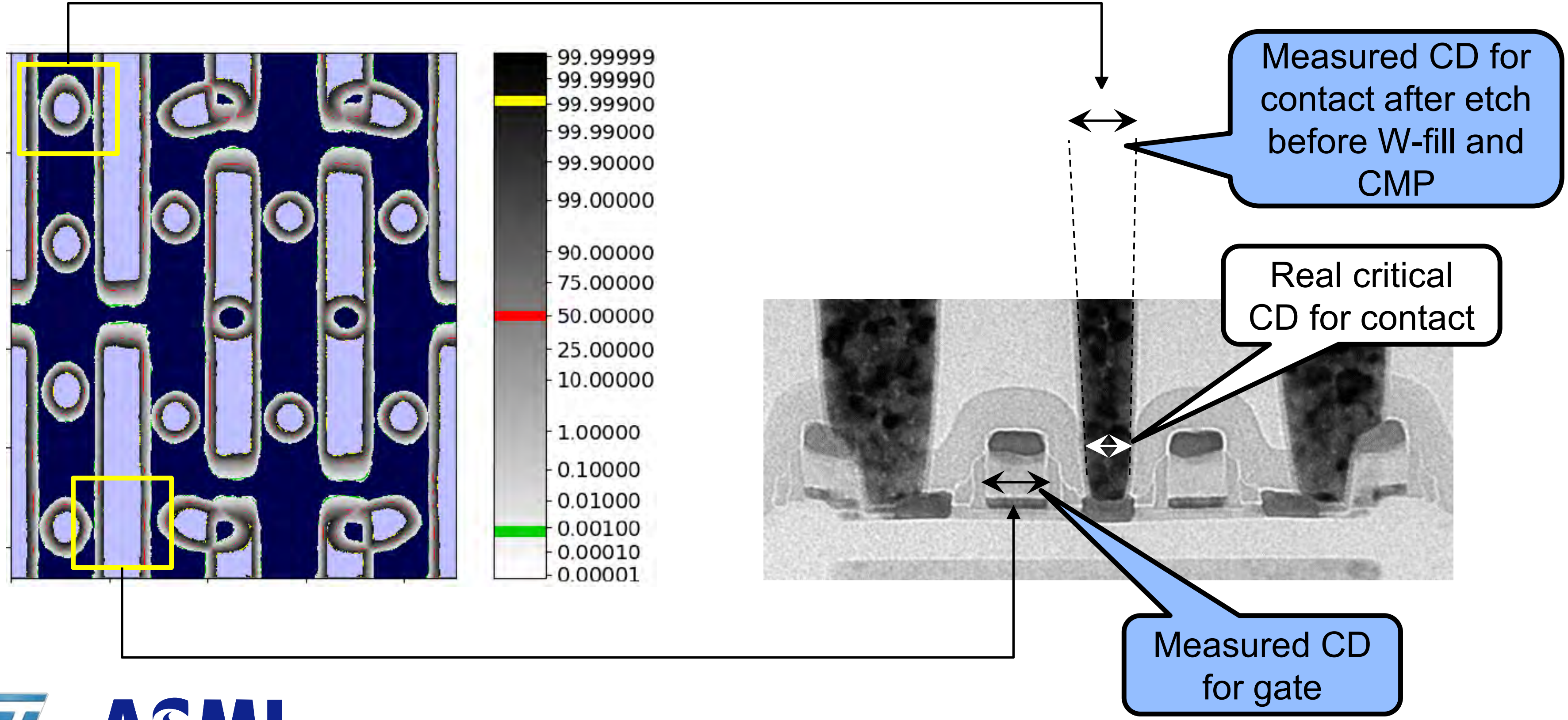




life.augmented

B Le-Gratiet et al, Proc. SPIE Vol. 10959 (2019)

EPE analysis - reminder

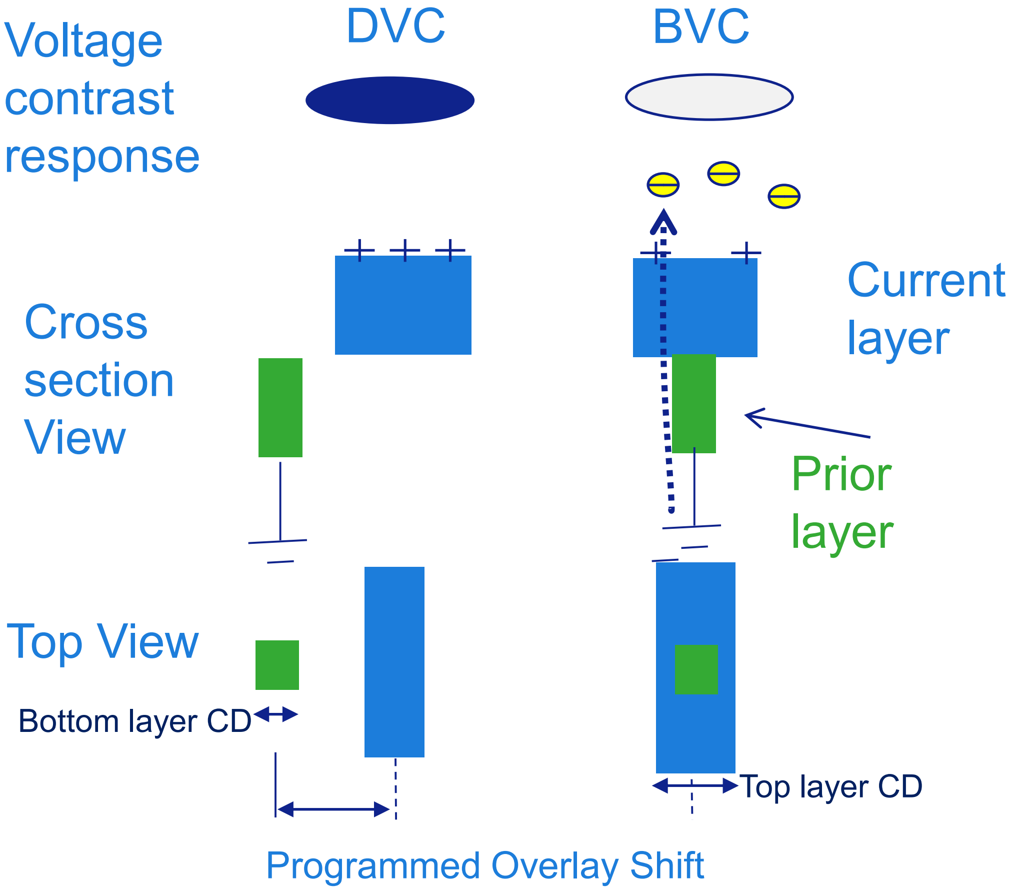


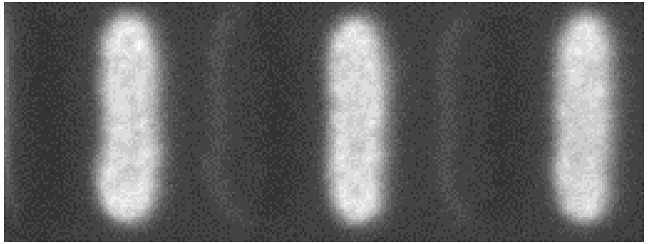
B Le-Gratiet et al, Proc. SPIE Vol. 10959 (2019)

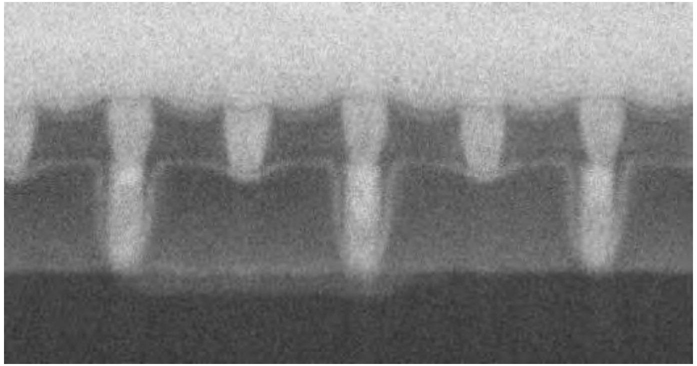
Public

Programmed overlay and CD variations modulate VC

Intra test mark design variation can allow EPE *inference* from VC signal







Floating metal is dark (DVC)

Grounded metal is bright (BVC)

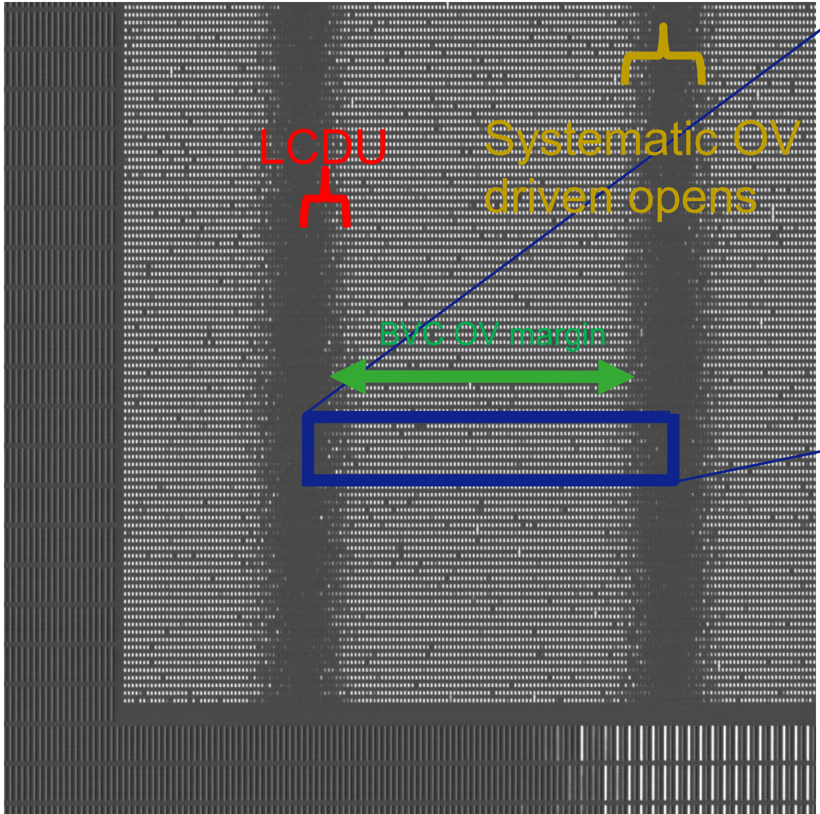
C.Tabery et al, Proc. SPIE Vol. 10959 (2019)

2 Layer continuously varying bias shows LCDU impact

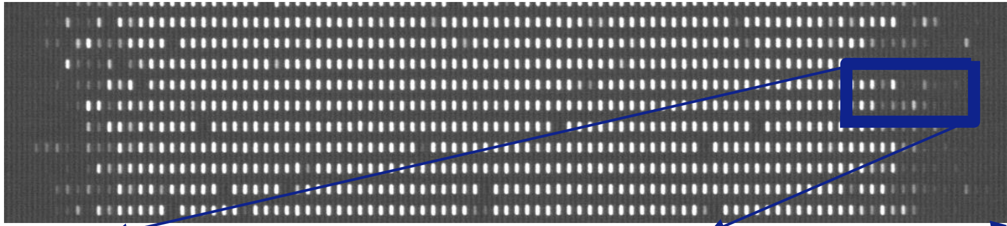
Pitch difference gives Moiré fringe Vernier with 1nm OV Steps

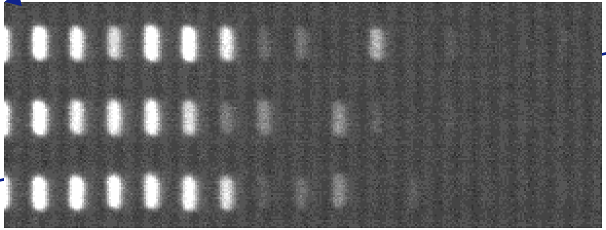
VC bit yield vs OV can be visualized directly with ebeam inspection image

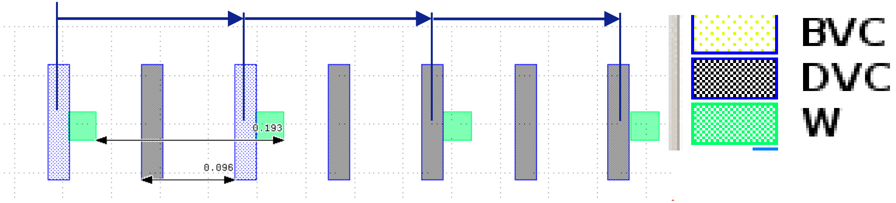
40 um FOV @10nm pixels



Note imperfect process with 2% yield loss @ PW center



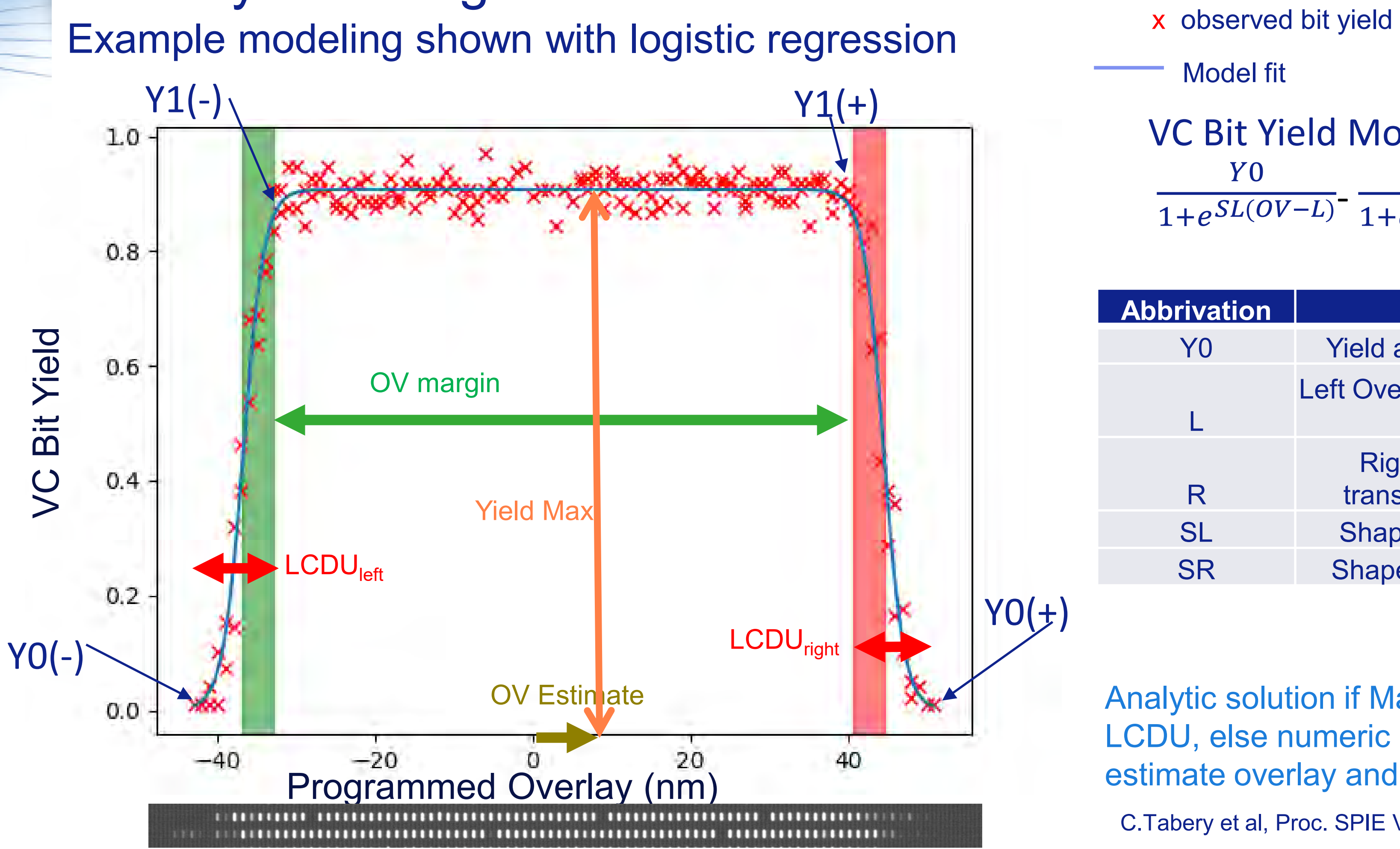




Top pitch 96nm, bottom pitch 193nm (2x+δ)

VC bit yield fitting enables EPE Estimation

Example modeling shown with logistic regression



$$\text{VC Bit Yield Model} = \frac{Y0}{1+e^{SL(OV-L)}} - \frac{Y0}{1+e^{SR(OV-R)}}$$

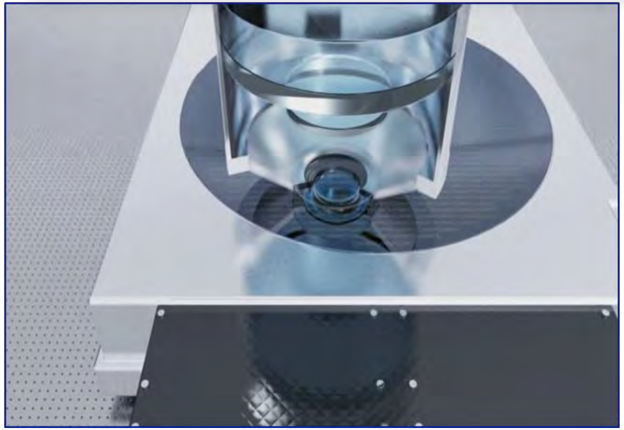
Abbrivation	Metric
Y0	Yield at PW center
L	Left Overlay transistion point
R	Right overlay transition point
SL	Shape factor left
SR	Shape factor right

Analytic solution if Margin >> LCDU, else numeric root finding to estimate overlay and OV margin.

C.Tabery et al, Proc. SPIE Vol. 10959 (2019)

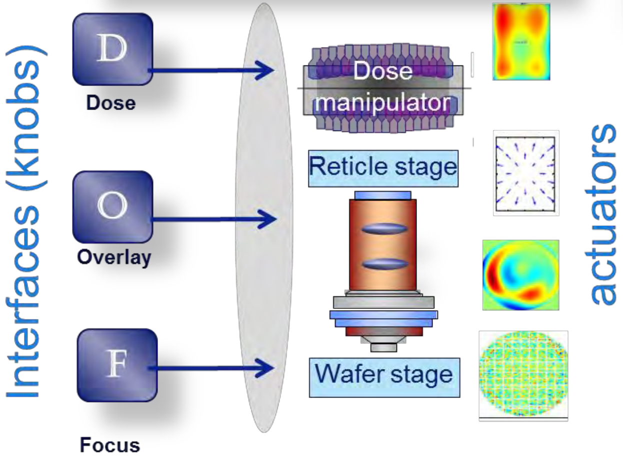
Lithography supports correction of the patterning at all length scales

Scanner exposure is field-by-field



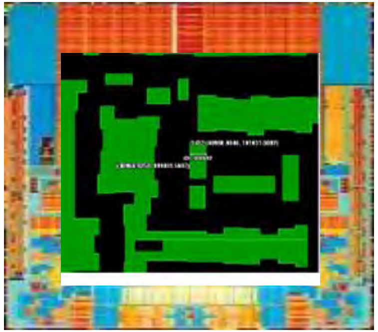
m-scale

Inside NXT and NXE scanners



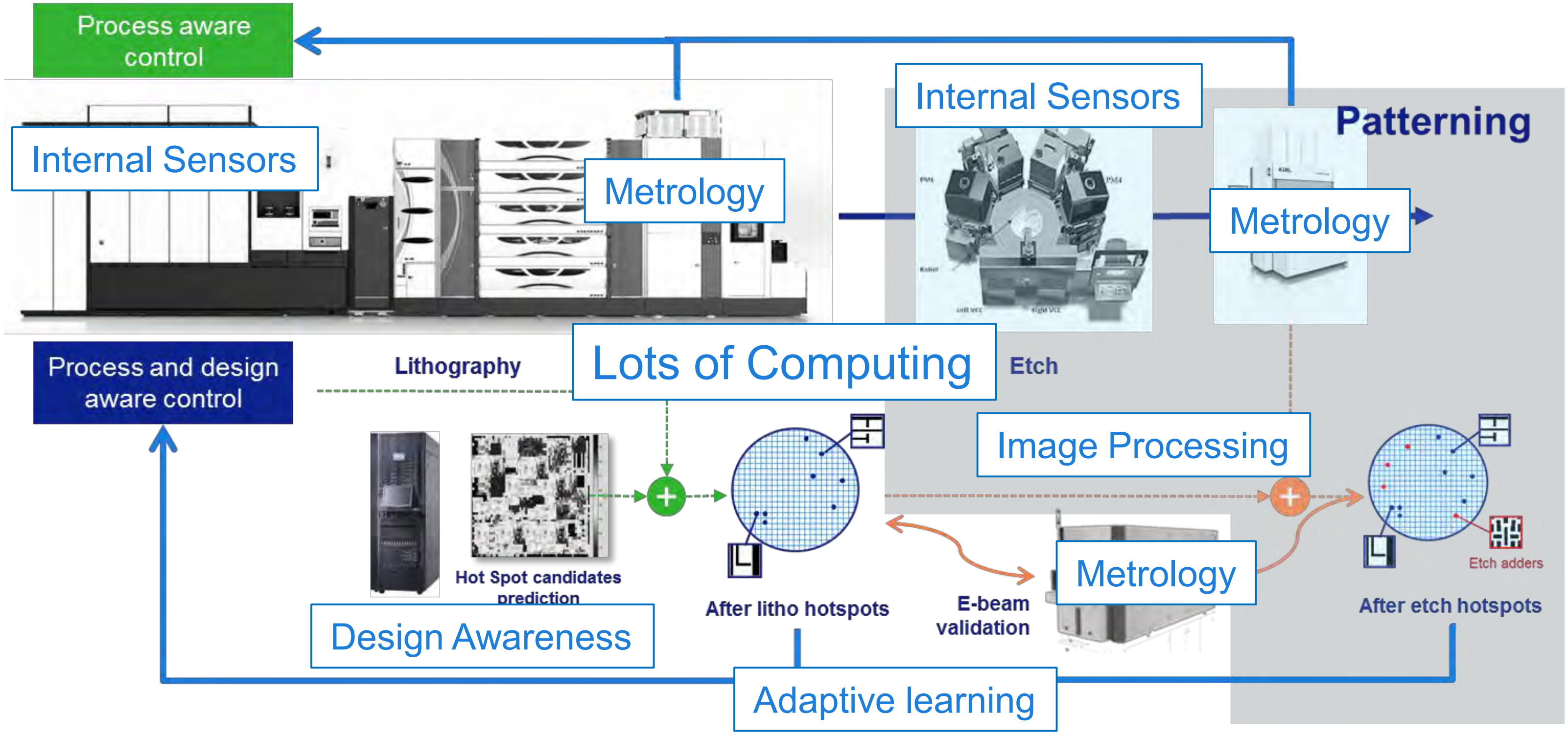
mm-scale

Feature-Scale Correction with OPC



nm-scale

Feedback and Feedforward



Measurements made at multiple steps in Patterning flow to enable optimal correction

Outline

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Conclusions

- Semiconductor Innovation Continues on Multiple Fronts
- Lithography tools continue to push resolution → $k_1 * \lambda / NA$
  - Combined with known Multiple Patterning Techniques ***resolution*** (min CD/Pitch) is not limiting
- EPE ***Control*** is key for HVM
  - Comprehensive EPE budget
    - Account for all contributors, length scales and frequency of occurrence
  - Design-Aware budgeting – not just generic features
- Fantastic challenges to create the tools, metrology, models and control systems to enable new technologies
- Need to create data analytics to support Real-Time, Design-Aware control of complete patterning process to meet EPE budgets

Acknowledgements

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