The Discussion of the Typical BEOL Design Rules from 3 nm to 2 nm Logic Process with EUV and High NA EUV Lithography

对应用极紫外和高数值孔径极紫外光刻工艺的3 nm到2 nm逻辑设计规则的讨论

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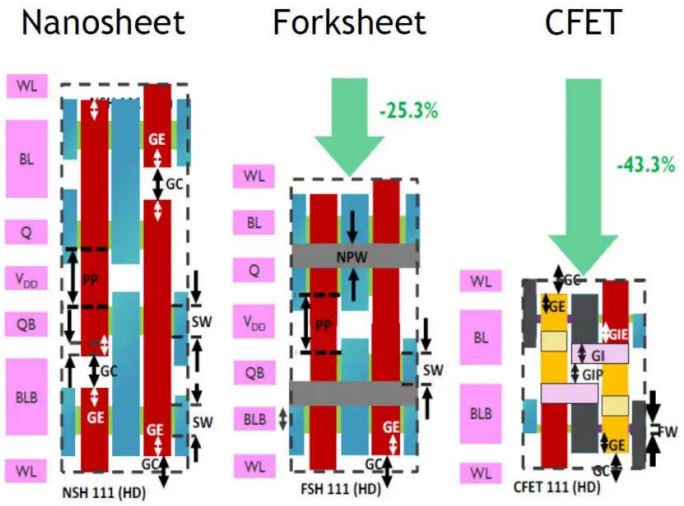
Outline

- Logic Design Rule Roadmaps
- Basic Design Rules for 3 nm Logic
- Basic Design Rules for 2 nm Logic
- Basic Design Rules for 1.5~1 Logic
- 0.33NA vs 0.55NA in cost for M1~M3
- A 3 nm CFET SRAM Design
- Process Window with 0.33NA EUV
- Process Window with 0.55NA EUV
- Conclusions and Summary

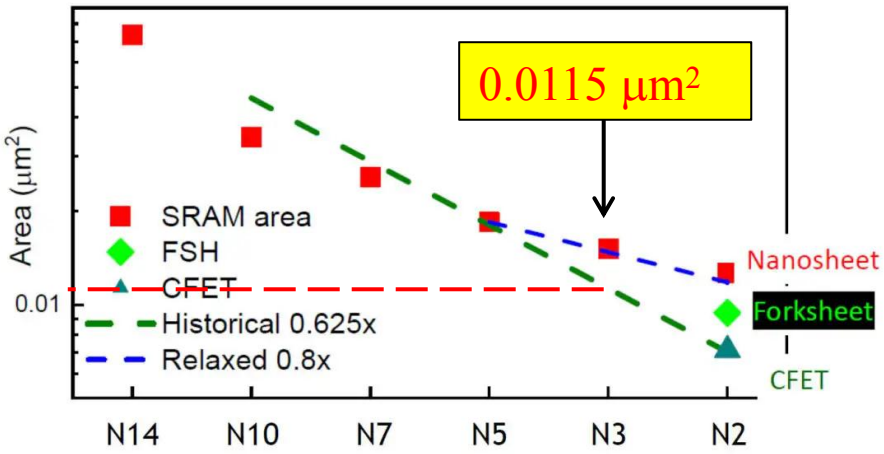
Logic Design Rule Roadmaps

SRAM area scaling: Nanosheet, Forksheet, CFET

HD SRAM bitcell design



HD SRAM area scaling



CFET can bring HD SRAM density scaling on track as compared to nanosheet

*Scotten Jones, "TSMC and IMEC on Advanced Process and Devices Technology Toward 2nm", VLSI Symposium 2021.

Logic Design Rule Roadmaps

Logic Tech Node	14 nm 2015	10 nm 2017	7 nm 2019	5 nm 2021	3 nm 2024	2.1 nm 2027	1.5 nm 2030	1.0 nm 2033
Fin Pitch（nm）	48 193i SADP	33 193i SAQP	27~30 193i SAQP	22.5~25 193i SAQP	20（？） 193i SAQP			
for Nano-plate/Nano-wires（nm）					21 193i SAQP	18 0.33NA EUV SADP	14 0.33NA EUV SAQP	14 0.33NA EUV SAQP
Gate Pitch（nm）	78/84~90 193i SP	66 193i SADP	54~58 193i SADP	48~50 193i SADP	36~42 193i SADP/SAQP	32 193 i SAQP，0.33NA EUV SADP	32 193 i SAQP，0.33NA EUV SADP	32 193 i SAQP，0.33NA EUV SADP
Metal Pitch（nm）	64 193i LE2	44 193i SALE2	40 193i SALE2/ 0.33NA EUVSP	30~32 0.33NA EUV SALE2	20~24 0.33NA EUV SALE2	14~18 0.55NA EUV SALE2	14 0.55NA EUV SALE2	14 0.55NA EUV SALE2
Via Pitch（nm）	64~80 193i LE2	44~62 193i LE2	40~56 193i LE3/ 0.33NA EUV SP	36~50 0.33NA EUV SP/LE2	30~36 0.33 NA EUV LE2	25 0.55 NA EUV LE3/ EUV+DSA	20 0.55 NA EUV LE4/ EUV+DSA	20 0.55 NA EUV LE4/ EUV+DSA

*“Chinas integrated circuit development roadmap”, National integrated circuit innovation center, 2019.

Basic Design Rules for 3 nm Logic

3 nm CFET BEOL（loose）

BEOL Layers	Pitch		Linewidth		Expo	Photolithography Method 0.33NA						Expo	Photolithography Method 0.55NA					
	Min Pitch (nm)	SE pitch (nm)	Min Pitch (nm)	SE pitch (nm)		Spec	TttT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)		Spec	TttT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)
Metal Layer	24	48/ 28*	12	24/ 14*	SALE2	Trgt	20	18	50	1.5	60	SALE 2	Trgt	16	18	40	1.5	60
	K1		0.586/ 0.57			Act	20	19.8	154	1.472	60		Act	16	17.7	42	1.69	58.6
Via Layer	36	48/ 36*	20	25/ 20*	LE2	Trgt		18	50	3.0	60	SE	Trgt		18	40	3.0	60
	K1		0.59/0.73			Act		21.5	105	2.31	60		Act		>30	46	1.3	42.9

* limited by EUV photon absorption stochastics

Basic Design Rules for 3 nm Logic

3 nm CFET BEOL（tight）

BEOL Layers	Pitch		Linewidth		Expo	Photolithography Method 0.33NA						Expo	Photolithography Method 0.55NA					
	Min Pitch (nm)	SE pitch (nm)	Min Pitch (nm)	SE pitch (nm)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)
Metal Layer	20	40/28*	10	21/14*	SALE2	Trgt	20	18	50	1.5	60	SALE2	Trgt	16	18	40	1.5	60
	K1		0.49/0.57		RDR**	Act	20	22.9 (14.8)**	>120	1.32 (1.89)**	60	NoRDR	Act	16	17.7	42	1.69	60
Via Layer	30	48/36*	16	25/20*	LE3	Trgt		18	50	3.0	60	LE2	Trgt		18	40	3.0	60
	K1		0.59/0.73		NoRDR	Act		21.5	105	2.31	60	NoRDR	Act		>30	46	1.3	42.9

* limited by EUV photon absorption stochastics
** indicates worst numbers across the pitches where the Restrictive Design Rules (RDR) may apply

Basic Design Rules for 2 nm Logic

2 nm CFET BEOL（loose）

BEOL Layers	Pitch		Linewidth		Expo	Photolithography Method 0.33NA						Expo	Photolithography Method 0.55NA					
	Min Pitch (nm)	SE pitch (nm)	Min Pitch (nm)	SE pitch (nm)		Spec	TtT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)		Spec	TtT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)
Metal Layer	18	36/28*	10	18/14*	SALE2	Trgt	20	18	50	1.5	60	SALE2	Trgt	16	18	40	1.5	60
	K1		0.44/0.57		RDR**	Act	20	18.2 (10.11)**	11 1.2	1.5 (2.55)**	60	No RDR	Act	16	17.7	42	1.69	62.4
Via Layer	25	48/36*	14	25/20*	LE 4~6	Trgt		18	50	3.0	60	LE 2~3	Trgt		18	40	3.0	60
	K1		0.59/0.73		No RDR	Act		21.5	103	2.31	60	No RDR	Act		>30	46	1.3	42.9

* limited by EUV photon absorption stochastics
** indicates worst numbers across the pitches where the Restrictive Design Rules (RDR) may apply

Basic Design Rules for 2 nm Logic

2 nm CFET BEOL（tight）

BEOL Layers	Pitch		Linewidth		Expo	Photolithography Method 0.33NA						Expo	Photolithography Method 0.55NA					
	Min Pitch (nm)	SE pitch (nm)	Min Pitch (nm)	SE pitch (nm)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm²)
Metal Layer	14	42/28*	8	21/14*	SALE 3	Trgt	20	18	50	1.5	60	SALE 2	Trgt	16	18	40	1.5	60
	K1		0.51/0.57		RDR in 2D	Act	20	22.9 (14.8) **	>120	1.32 (1.89) **	60	No RDR	Act	16	17.7	42	1.69	62.4
Via Layer	25	48/36*	14	25/20*	LE 4~6	Trgt		18	50	3.0	60	LE 2~3	Trgt		18	40	3.0	60
	K1		0.59/0.73		No RDR	Act		21.5	103	2.31	60	No RDR	Act		>30	46	1.3	42.9

* limited by EUV photon absorption stochastics

** indicates worst numbers across the pitches where the Restrictive Design Rules (RDR) may apply

Basic Design Rules for 1.5~1 nm Logic

1.5~1 nm CFET BEOL

BEOL Layers	Pitch		Linewidth		Expo	Photolithography Method 0.33NA						Expo	Photolithography Method 0.55NA					
	Min Pitch (nm)	SE pitch (nm)	Min Pitch (nm)	SE pitch (nm)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm^2)		Spec	T tT (ADI, nm)	EL (%)	DoF (nm)	MEF	E (mj/cm^2)
Metal Layer	14	42/28*	8	21/14*	SALE3	Trgt	20	18	50	1.5	60	SALE2	Trgt	16	18	40	1.5	60
	K1		0.51/0.57		RDR	Act	20	22.9 (14.8) **	>120	1.32 (1.89) **	60	NoRDR	Act	16	17.7	42	1.69	62.4
Via Layer	20	48/36*	12	25/20*	LE6~9	Trgt		18	50	3.0	60	LE3~4	Trgt		18	40	3.0	60
	K1		0.59/0.73		NoRDR	Act		21.5	103	2.31	60	NoRDR	Act		>30	46	1.3	42.9

* limited by EUV photon absorption stochastics
** indicates worst numbers across the pitches where the Restrictive Design Rules (RDR) may apply

0.33NA vs 0.55NA in cost for M1~M3

- Assuming 0.33NA EUV cost takes ~45% of the total process cost
- Assuming 0.55NA EUV costs about 2X as much as the 0.33NA
- Total cost is estimated for M1~M3 layers

- It seems that starting at the 2 nm mode, the 0.55NA EUV cost will be lower than that of the 0.33NA.

3 nm					
0.55NA/0.33NA cost ratio			2		
0.33NA Layers	16		0.55NA Layers	14	
	Cost/ layer	Cost for all layers		Cost/ layer	Cost for all layers
Expsure cost (0.33NA)	45	720	Expsure cost (0.55NA)	90	1260
Other process cost	55	880	Other process cost	55	770
Total cost		1600	Total cost		2030

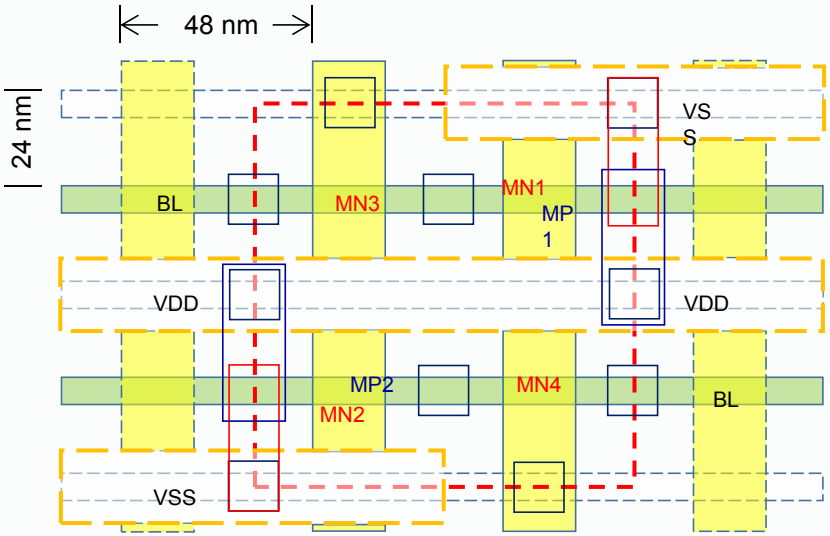
2 nm					
0.55NA/0.33NA cost ratio			2		
0.33NA Layers	25		0.55NA Layers	15	
	Cost/ layer	Cost for all layers		Cost/ layer	Cost for all layers
Expsure cost (0.33NA)	45	1125	Expsure cost (0.55NA)	90	1350
Other process cost	55	1375	Other process cost	55	825
Total cost		2500	Total cost		2175

1.5~1 nm					
0.55NA/0.33NA cost ratio			2		
0.33NA Layers	30		0.55NA Layers	17	
	Cost/ layer	Cost for all layers		Cost/ layer	Cost for all layers
Expsure cost (0.33NA)	45	1350	Expsure cost (0.55NA)	90	1530
Other process cost	55	1650	Other process cost	55	935
Total cost		3000	Total cost		2465

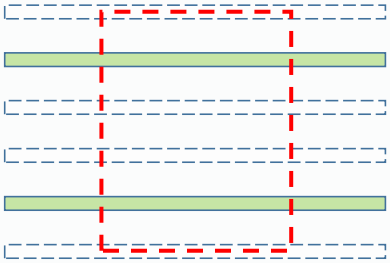
A 3 nm CFET SRAM Design

- A 3 nm CFET SRAM cell design with relatively “loose” design rule
- The Fin and Gate layers are made with 193 nm SAMP
- the metal layers are made with 0.33NA EUV SALE2 process (with cut)
- the via layers are made with 0.33NA EUV LE2 process

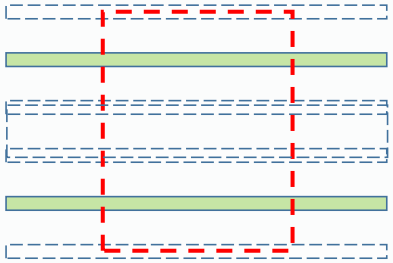
Area: 0.0115 μm²



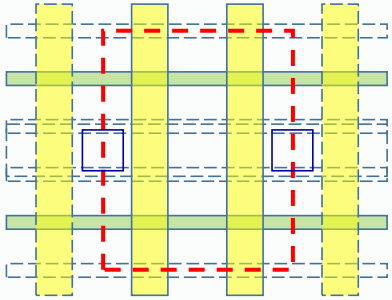
A 3 nm CFET SRAM Design



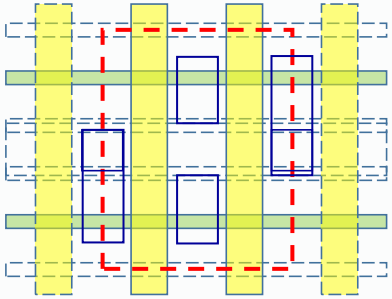
Fin + Cut



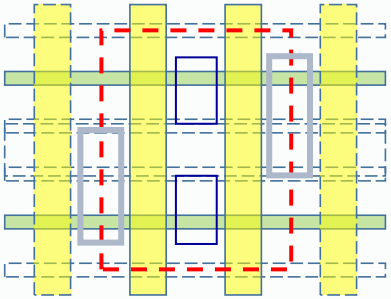
VDD BPR



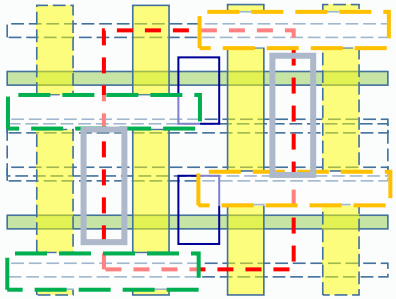
BPR CT， Poly，
Spacer



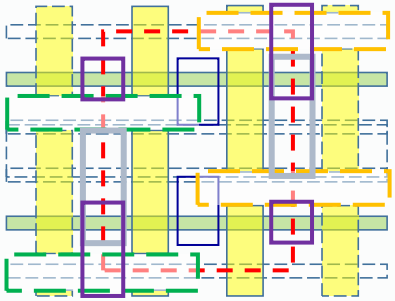
M0，PMOS/NMOS Epi



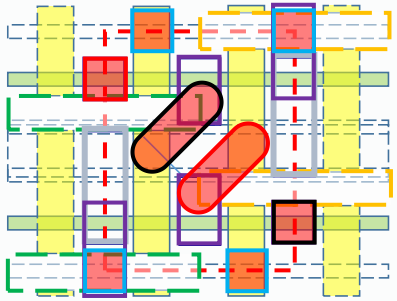
ILD，MG



P2

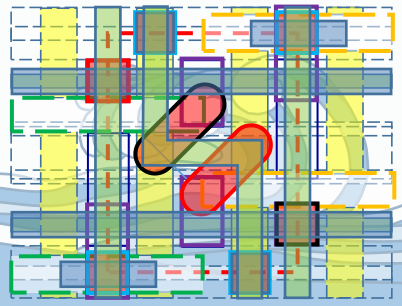


M0B



V0

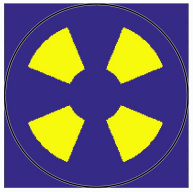
M1~V1~M2

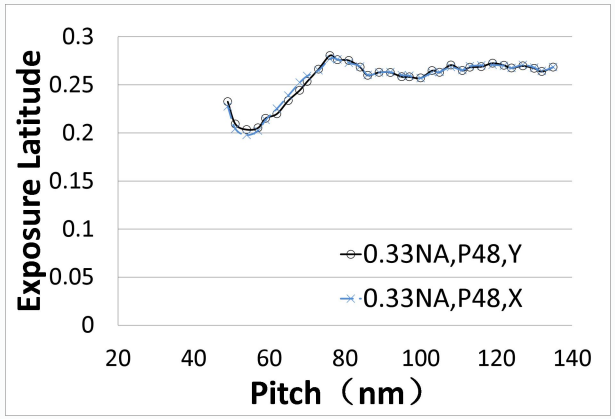


Process Window with 0.33NA EUV

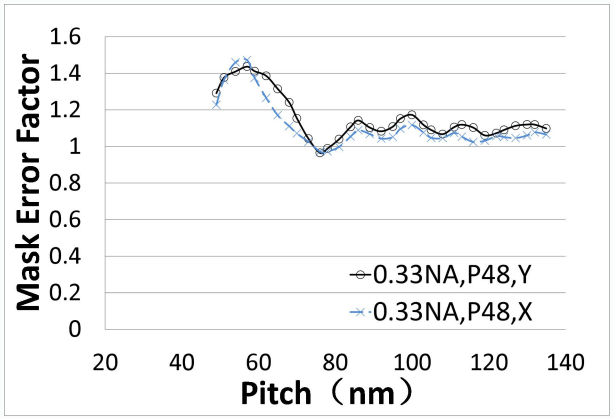
Metal Lithography：0.33NA

K1：0.586
P（min）=48 nm
Trench CD=24 nm
LWR(unbiased)=2.7 nm

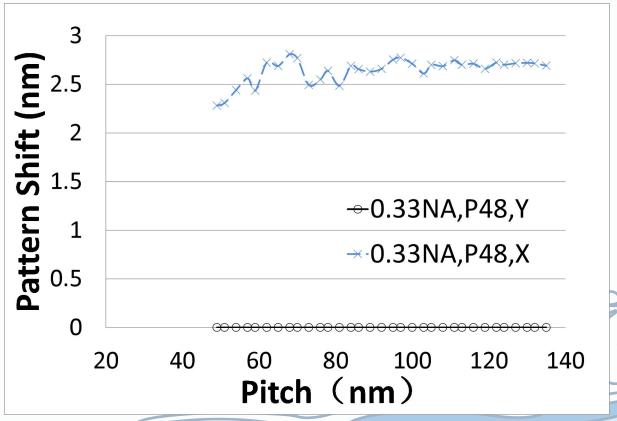




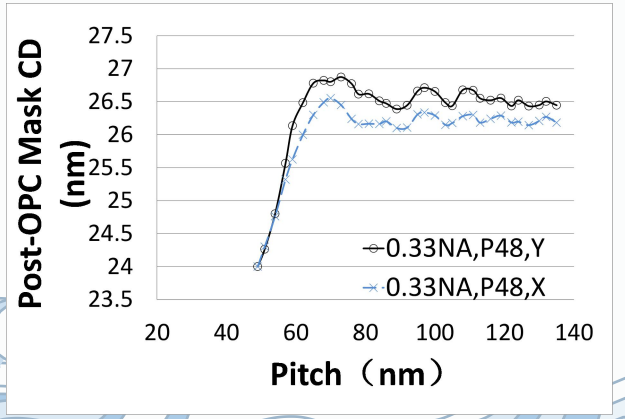
(a)



(b)



(c)

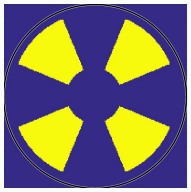


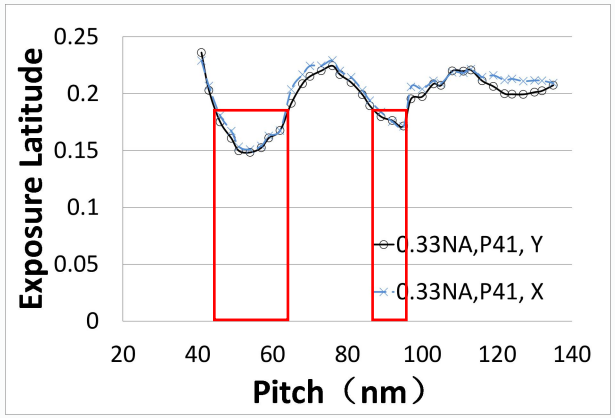
(d)

Process Window with 0.33NA EUV

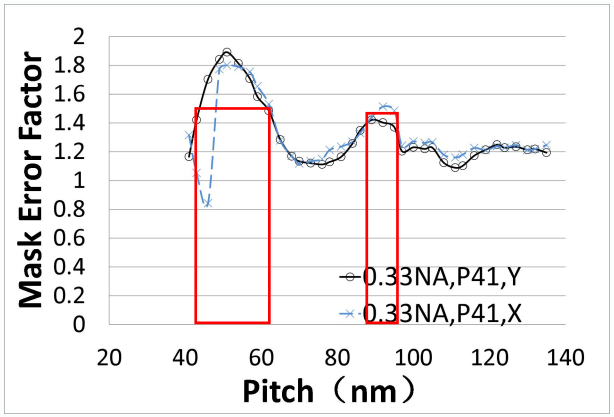
Metal Lithography：0.33NA

K1：0.50
P（min）=40 nm
Trench CD=21 nm
LWR(unbiased)=2.7 nm

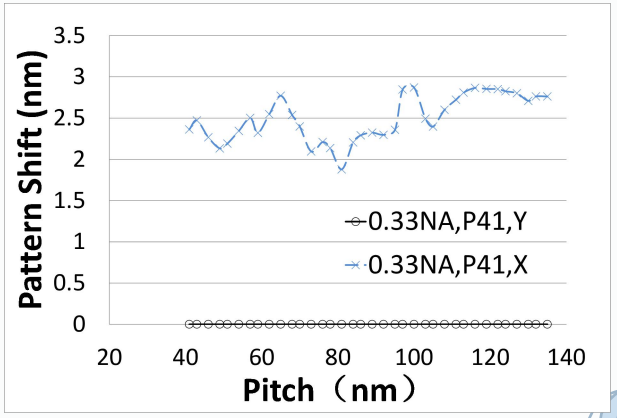




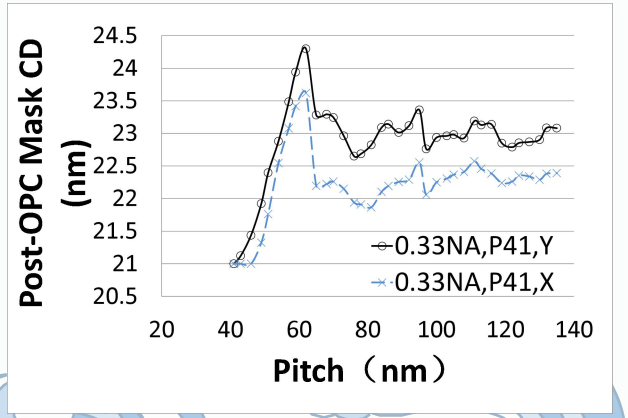
(a)



(b)



(c)

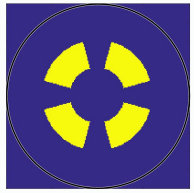


(d)

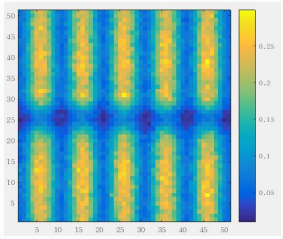
Process Window with 0.55NA EUV

Metal Lithography：0.55NA

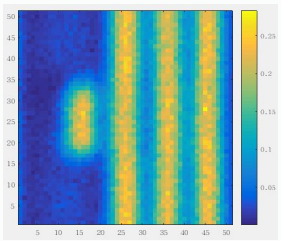
K1：0.57
P（min）=28 nm
Trench CD=14 nm
LWR(unbiased)=2.1 nm

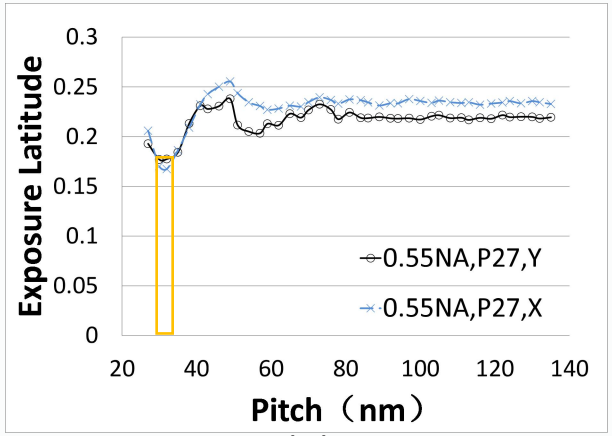


(e)*

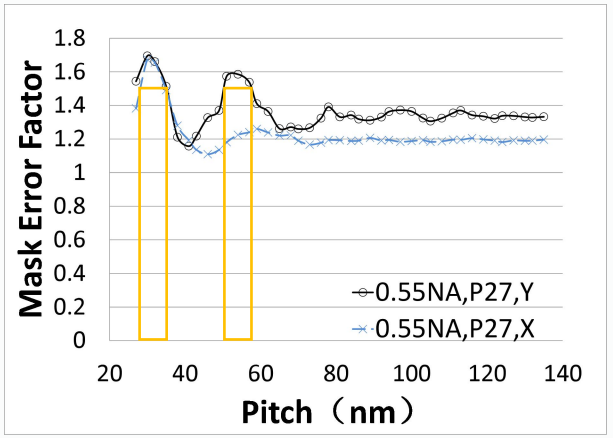


(f)*

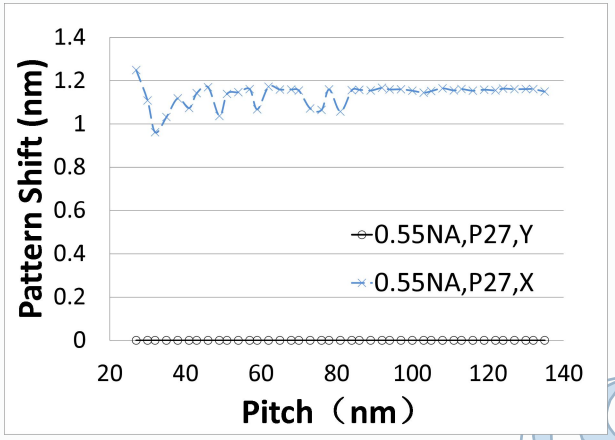




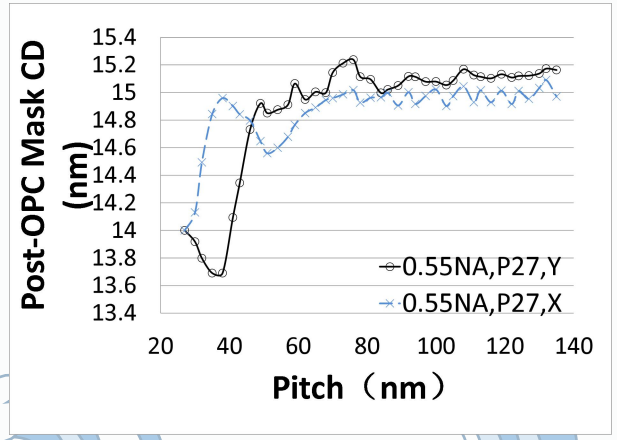
(a)



(b)



(c)



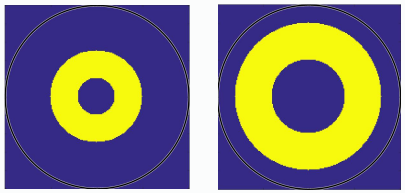
(d)

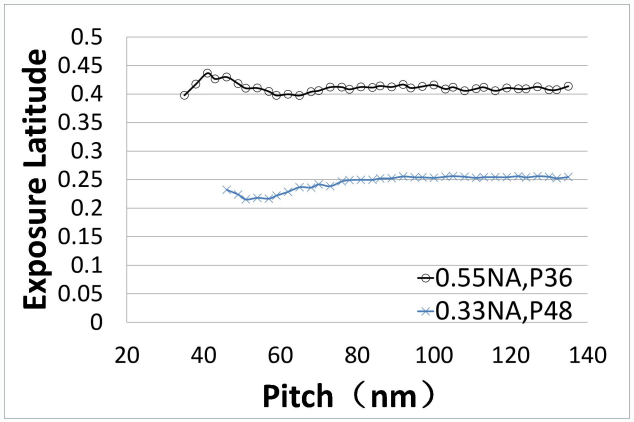
* Yanli Li et. al., IWAPS 2021

Process Window with 0.55NA EUV

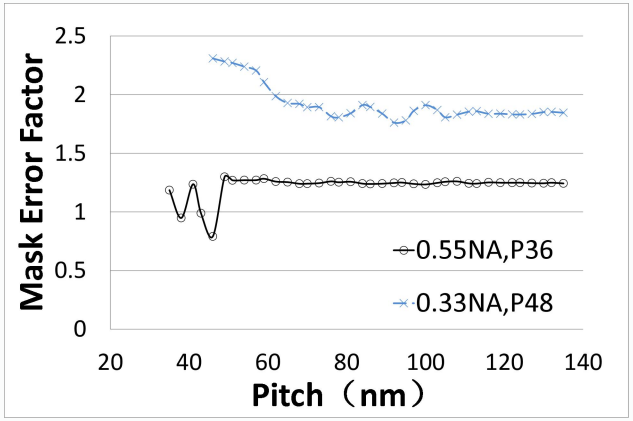
CT/Via Lithography：0.55NA vs. 0.33NA

K1：0.73/0.59
P（min）=36 nm/48 nm
CT/Via CD=20 nm/25 nm
LWR(unbiased)=2.1 nm/2.7 nm

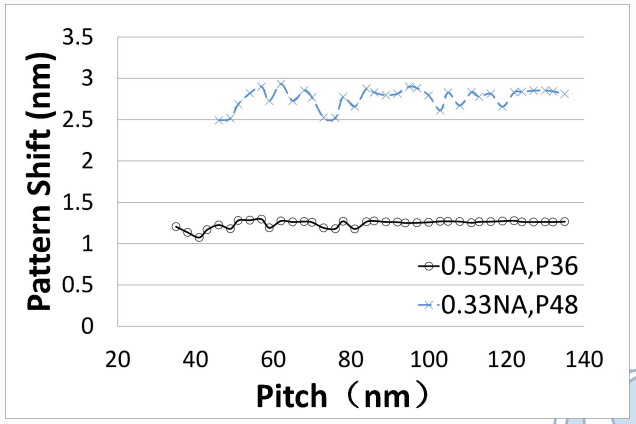




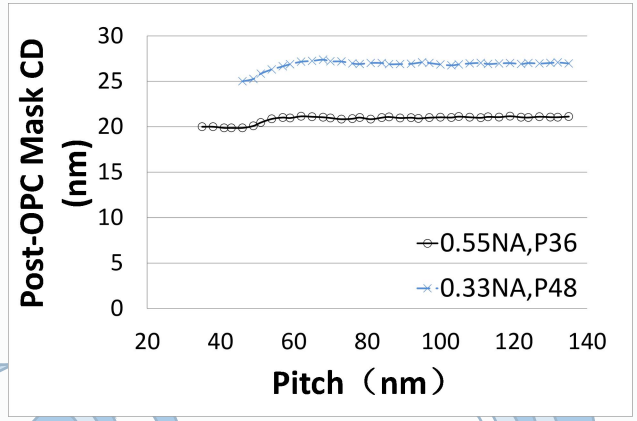
(a)



(b)



(c)



(d)

Conclusions and Summary

- We have done a study of the logic 3 nm and 2 nm design rules with a CFET SRAM design.
- We have studied the BEOL metal and via layers with both 0.33NA and 0.55NA EUV lithography process with a self-developed simulation model.
- With the simulation study, we have put together a simple calculation on the process cost for the metal 1 through metal 3 layers. We have confirmed that for the 3 nm technology node, the 0.33NA EUV is the cost effective way to go while at 2 nm and beyond, the 0.55NA EUV is a more viable solution.


谢谢！
我们的目标是星辰大海，诗和远方。。。。。。