

**IWAPS
2020**

International Workshop on

Advanced Patterning Solutions



国际先进光刻技术研讨会

2020年11月5日-6日
中国·成都

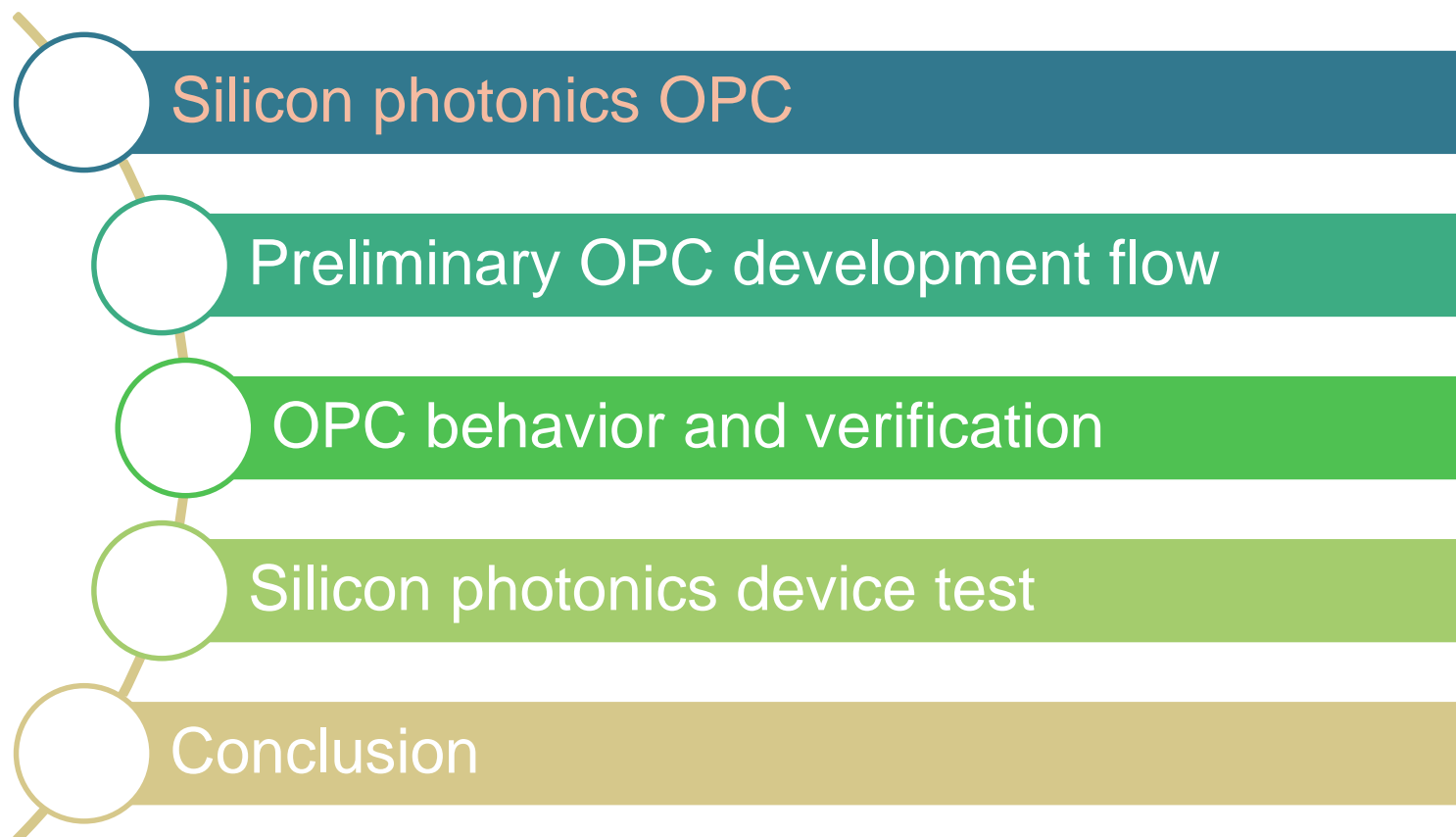
Preliminary Round of OPC Development in 180nm node Silicon Photonics MPW platform

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United Microelectronics Center Corporation ● Chongqing ● China

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Silicon photonics technology



optical transceiver



LiDAR

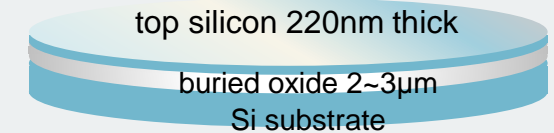
Si photonics design companies (many)

Intel, IBM, Mellanox, Rockley, Micron, NTT, Huawei, ZTE, Accelink...

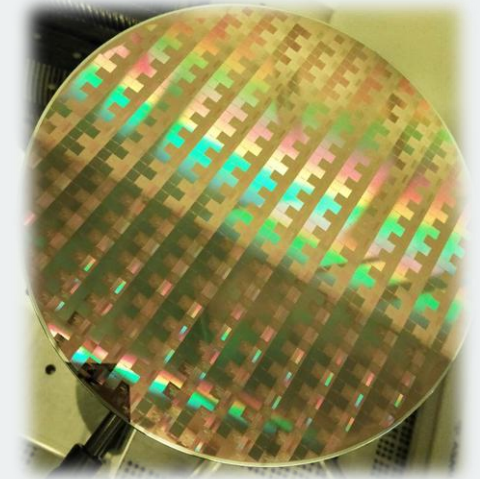


Foundries (few)

STM, Global foundries, AIM, Towerjazz, IMECAS,...



CMOS technology compatible



CUMEC—an emerging silicon photonics platform @ Chongqing, China

IWAPS
2020



2018.10
CUMEC founded

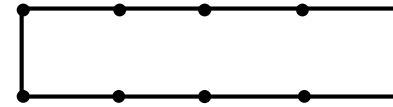
2019.8
8' silicon photonics line was ready

2020.5
CSiP180AL silicon photonics platform
180nm Si photonics PDK released

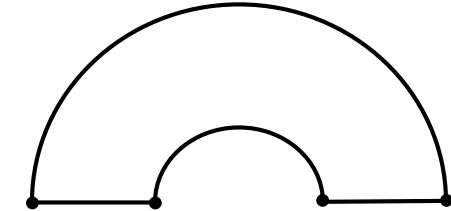
Silicon photonics OPC problems

Challenges

- Curvilinear pattern structures



Manhattan patterns



non-Manhattan(curvilinear)

- Multiple CD targets and varied types: isolate/dense, line/space

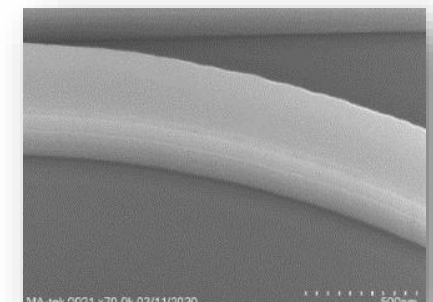
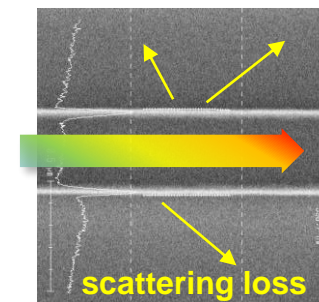
structures	size	type
waveguide	380/450nm	line
edge coupler	140nm	line
directional coupler	150-250nm	space

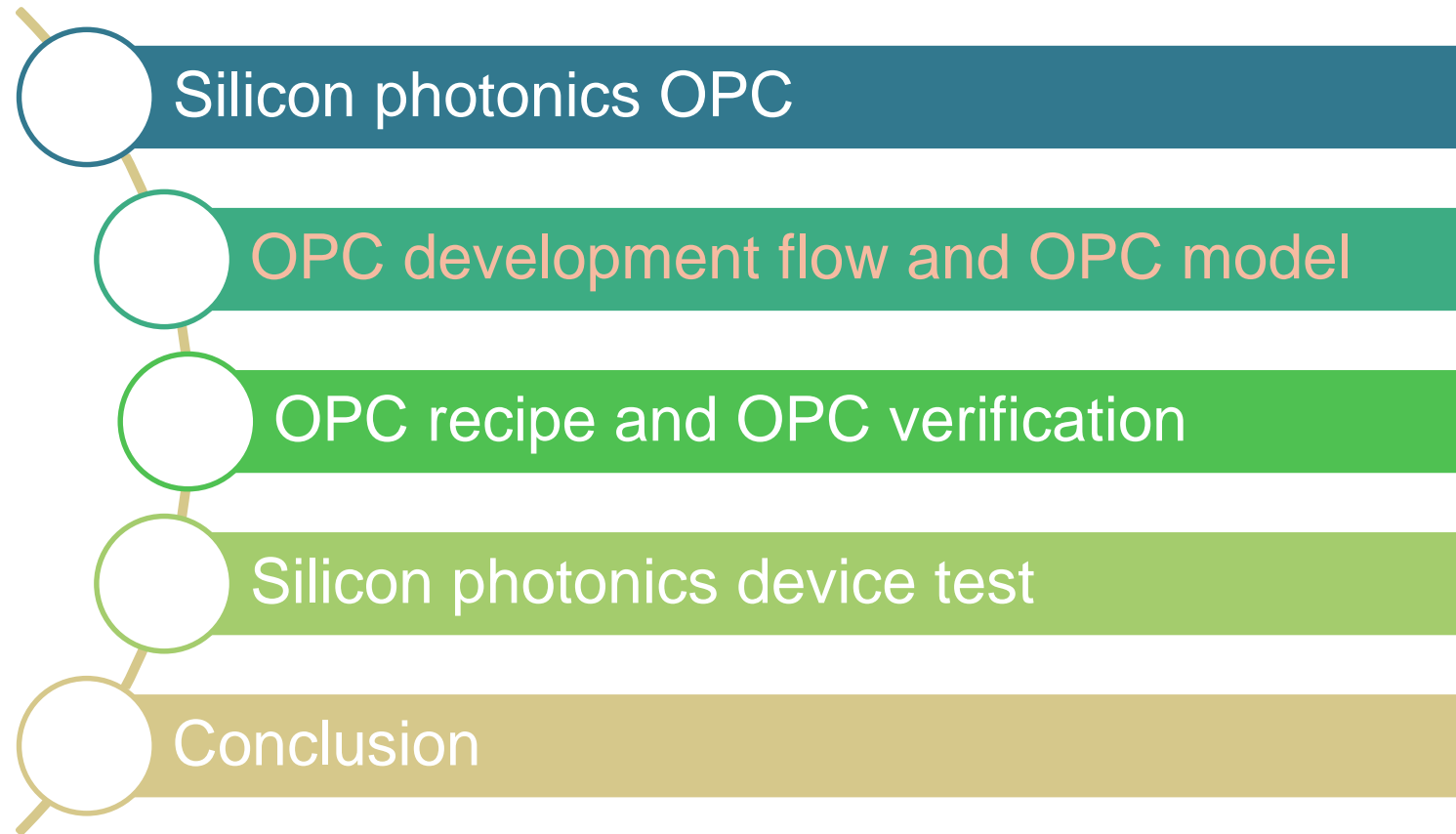
- Sidewall roughness should be considered

For a straight waveguide, Payne-Lacey transmission loss α in dB/cm

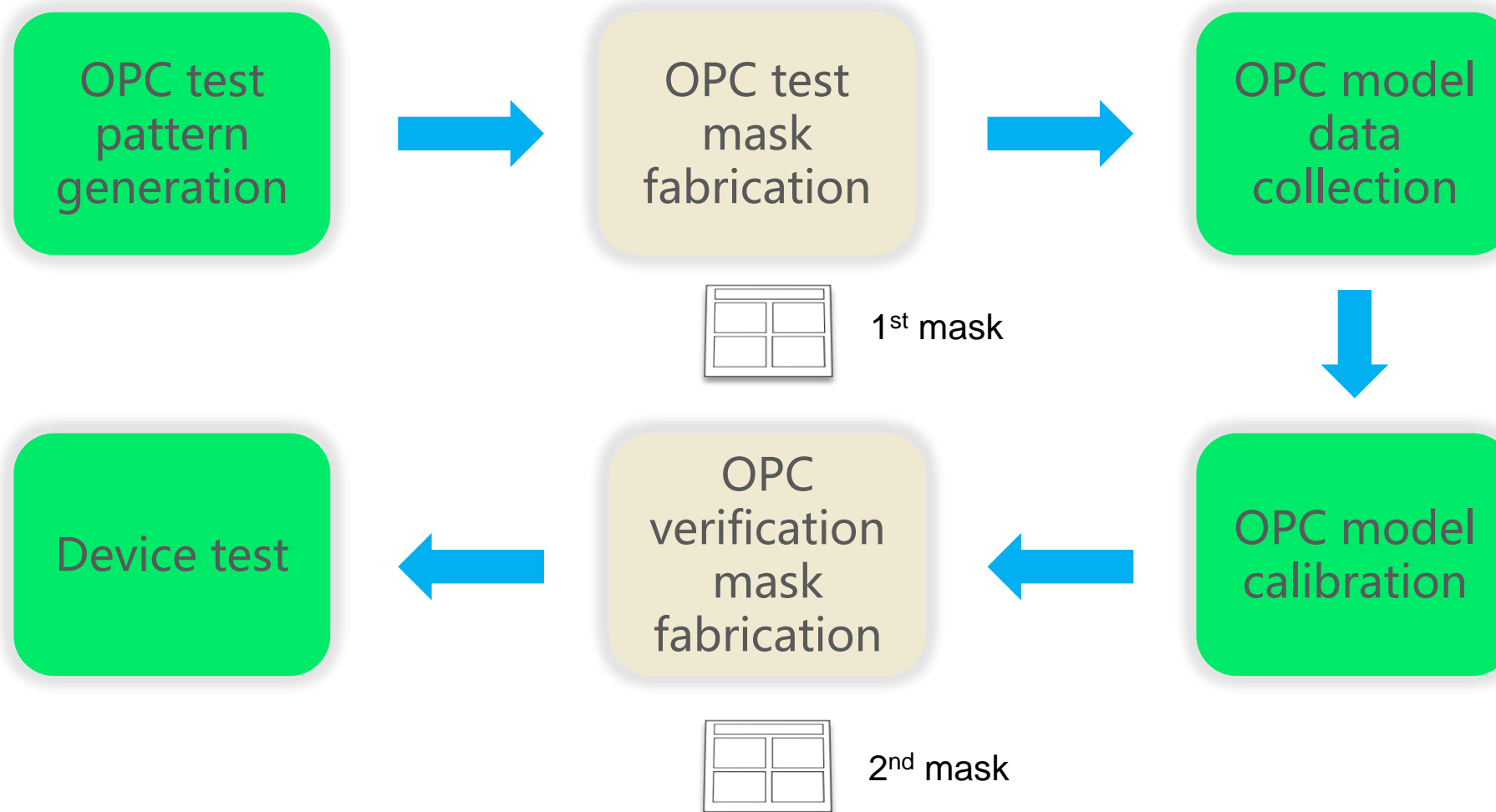
$$\alpha = \frac{\sigma^2}{\sqrt{2}k_0d^4n_1}gf_e$$

σ is the Root Mean Square (RMS) roughness of the waveguide.

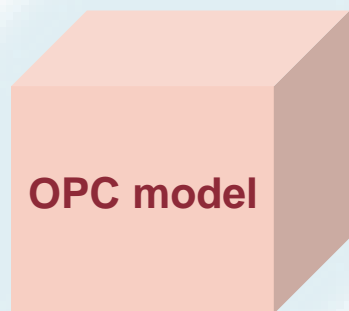




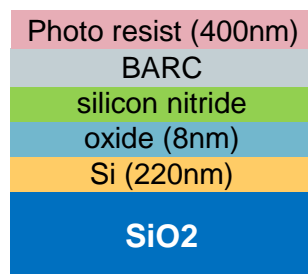
OPC development flow



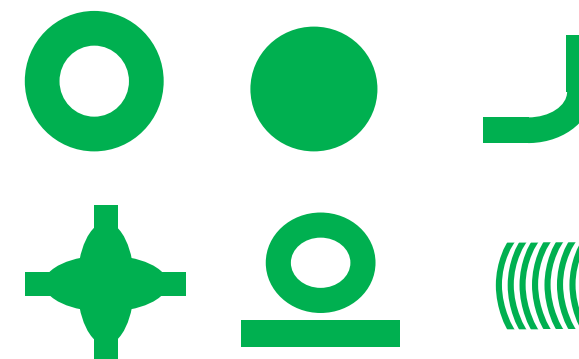
Si photonics test patterns



source wavelength: 248nm (KrF)
source type: annular
sigma /sigma in
film stacks information



1D/2D test patterns



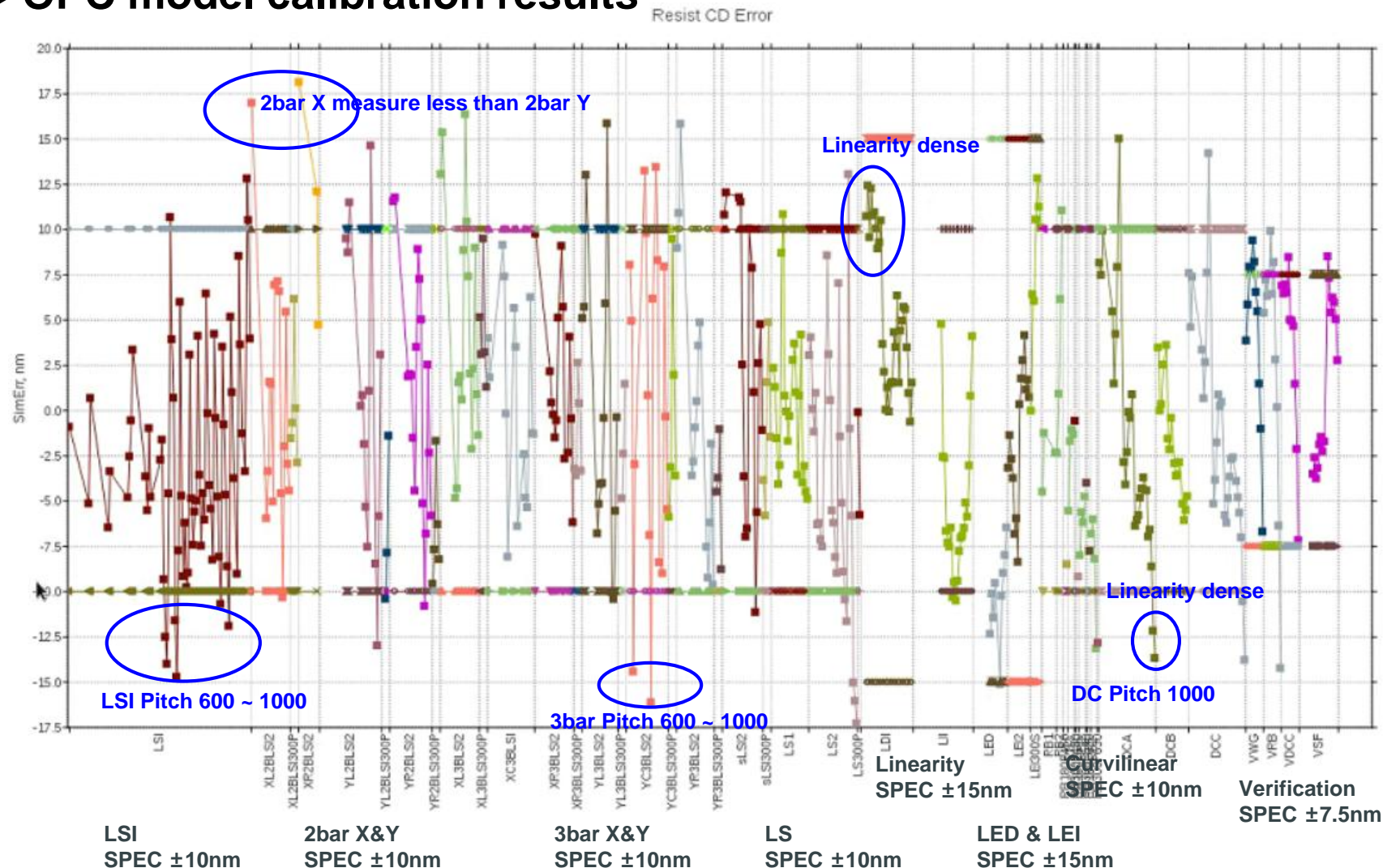
Curvilinear test patterns



silicon photonics real design
devices

OPC model Calibration

➤ OPC model calibration results

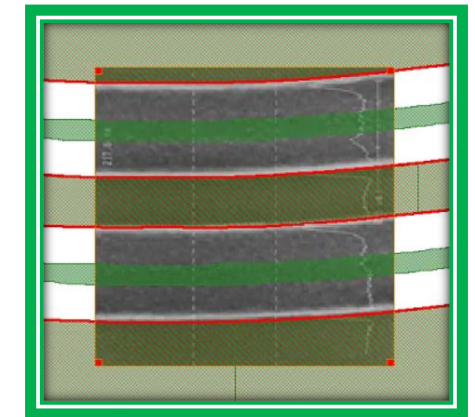
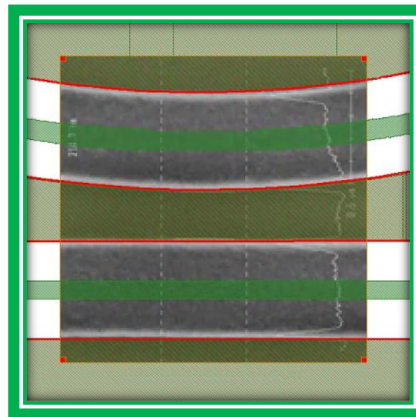
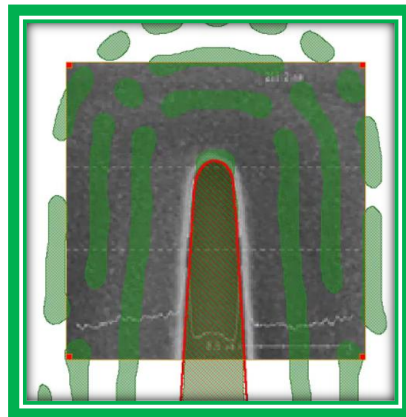
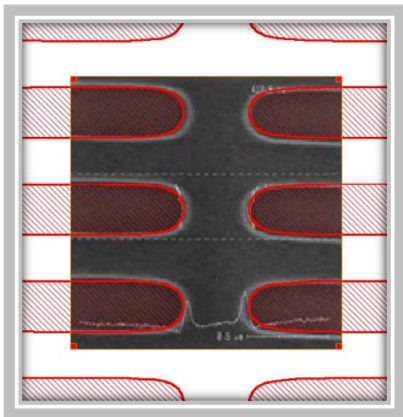
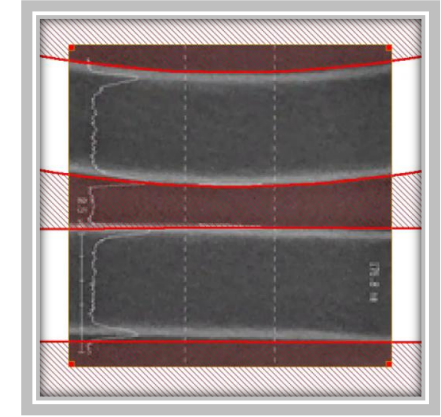
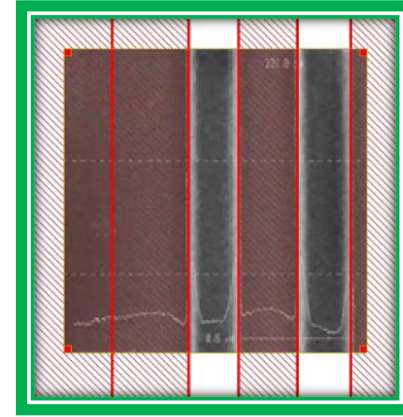
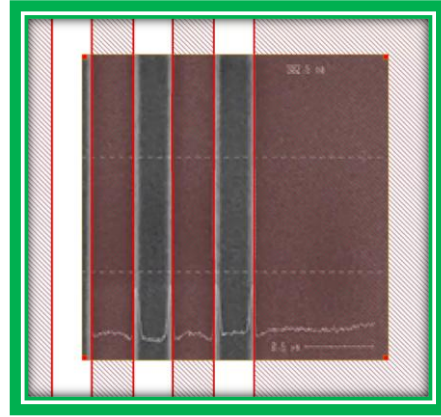
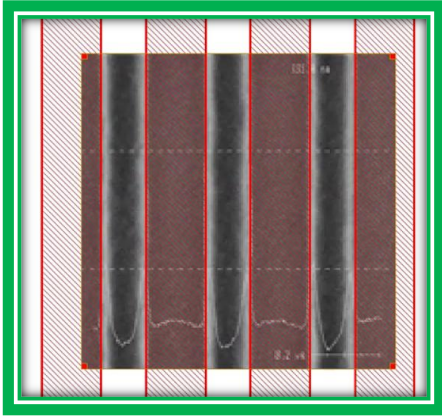


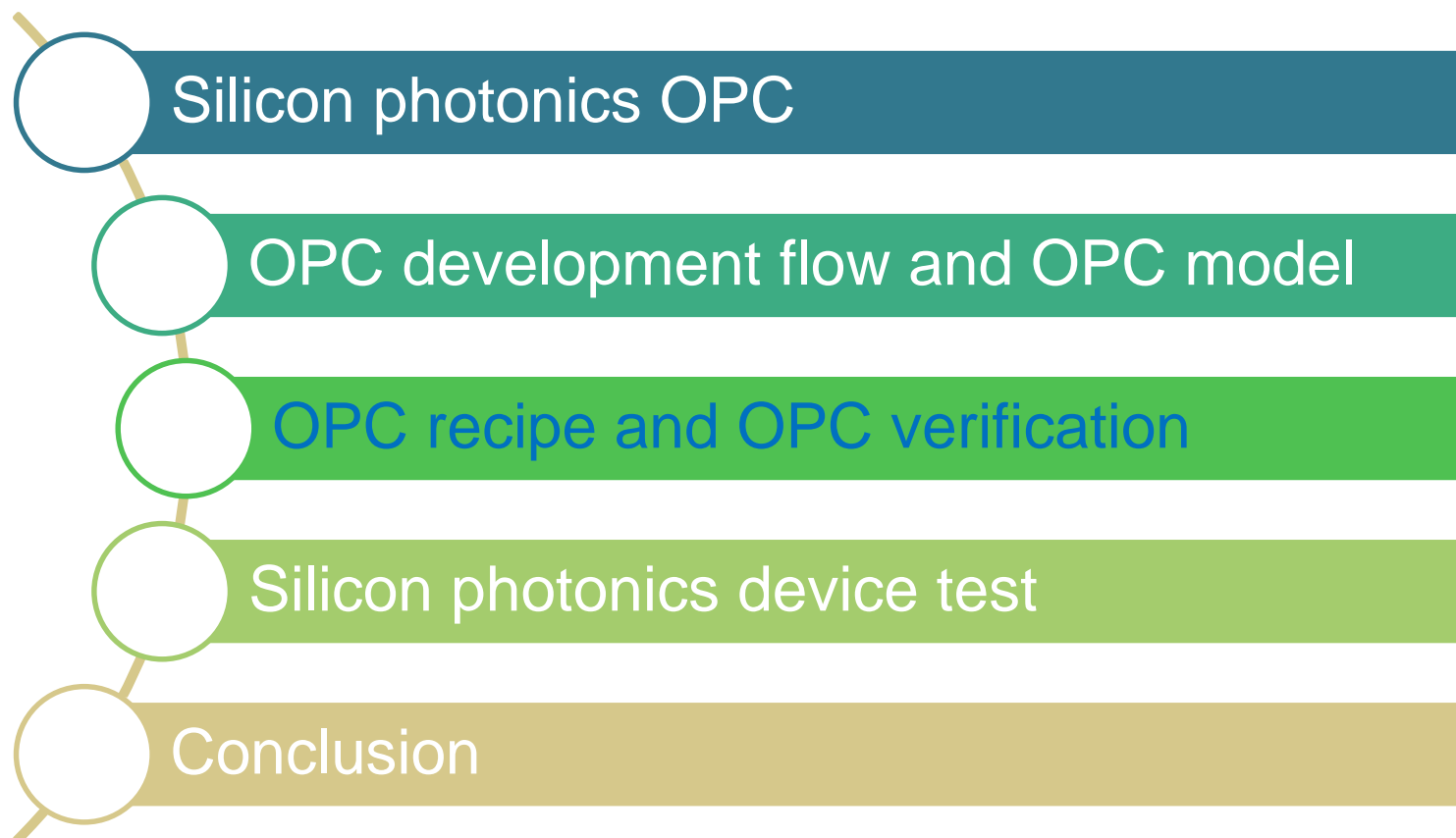
Anchor Results

	Dense150nm	380nm waveguide	450 nm waveguide
Target	130 \pm 10	415 \pm 10	490 \pm 10
Simulation	130.103	412.843	488.782
SimErr	0.103	-2.157	-1.218

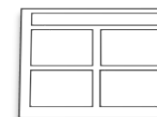
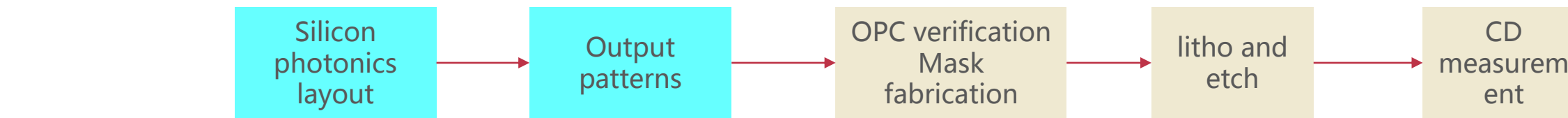
- In this calibration , pitch 600 ~ 1000nm was a trade off compare with anchor, to keep the anchor accurate, few shapes were out of SPEC.

OPC model verification





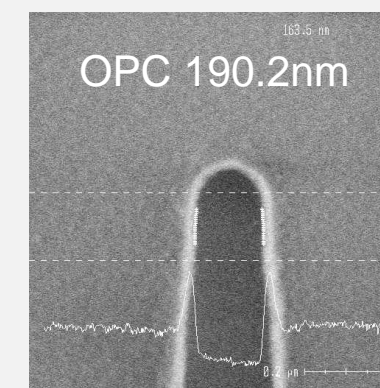
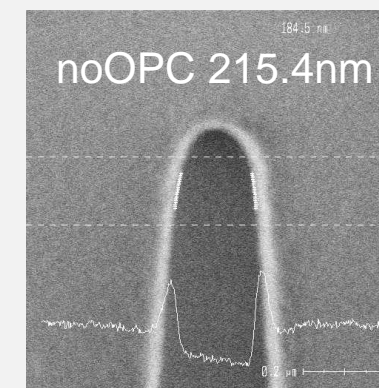
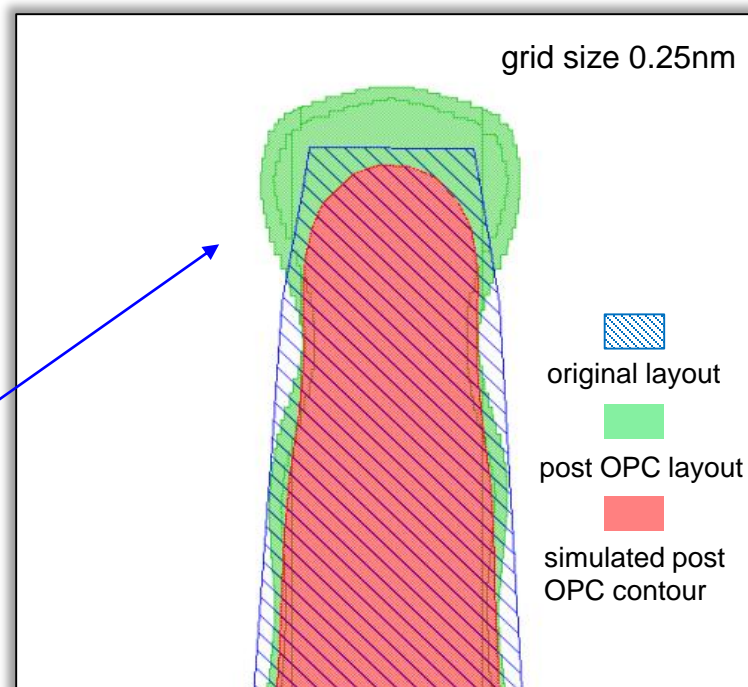
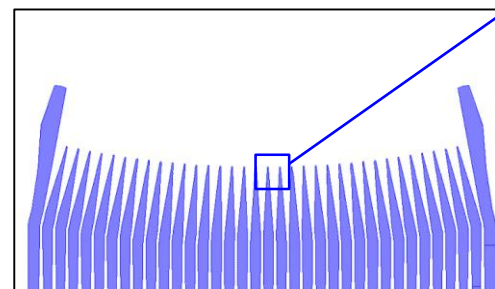
OPC verification (hotspots check)—AWG tips



2nd mask

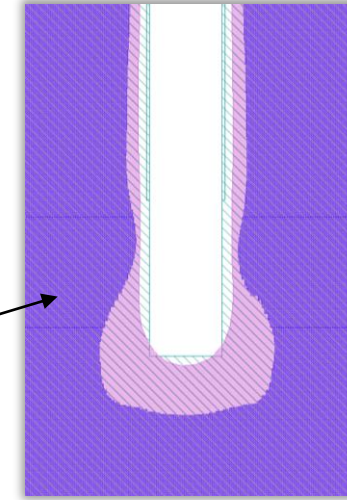
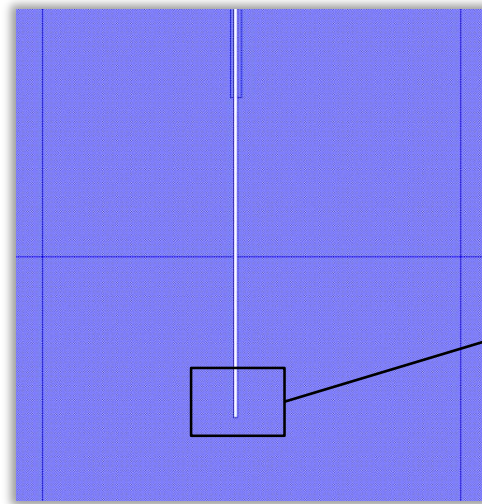
structure	AWG tip
isolated/dense	Isolated
line/space	space
designed CD	150 nm
AEI CD (noOPC)	215.4 nm
AEI CD (OPC)	190.2 nm




AWG-array waveguide grating

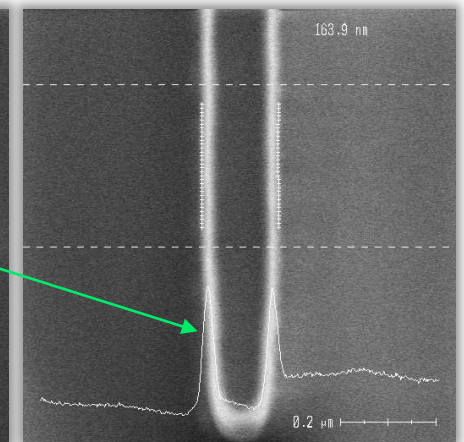
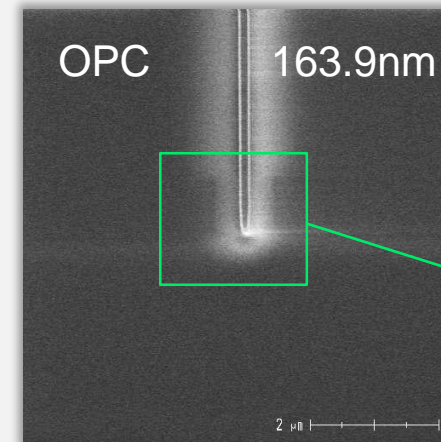
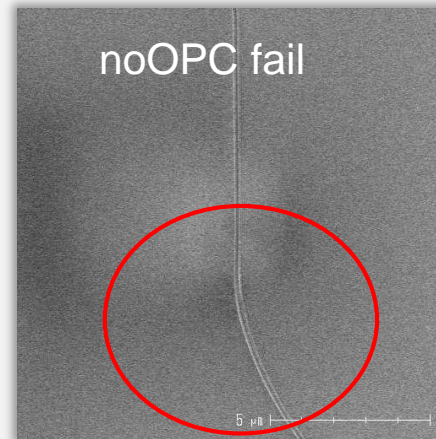


Hotspots check—140 nm edge coupler

structure	edge coupler
isolated/dense	Isolated
line/space	line
designed CD	140 nm
AEI CD (noOPC)	fail
AEI CD (OPC)	163.9 nm



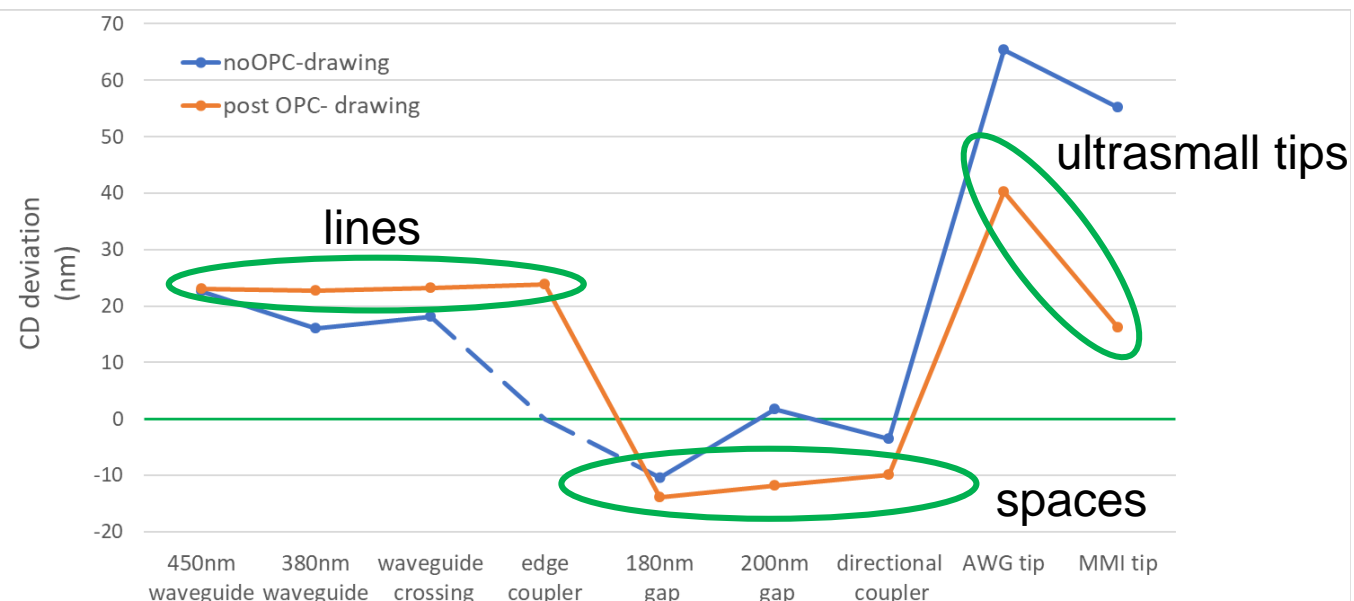
-  original layout
-  post OPC layout
-  simulated contour

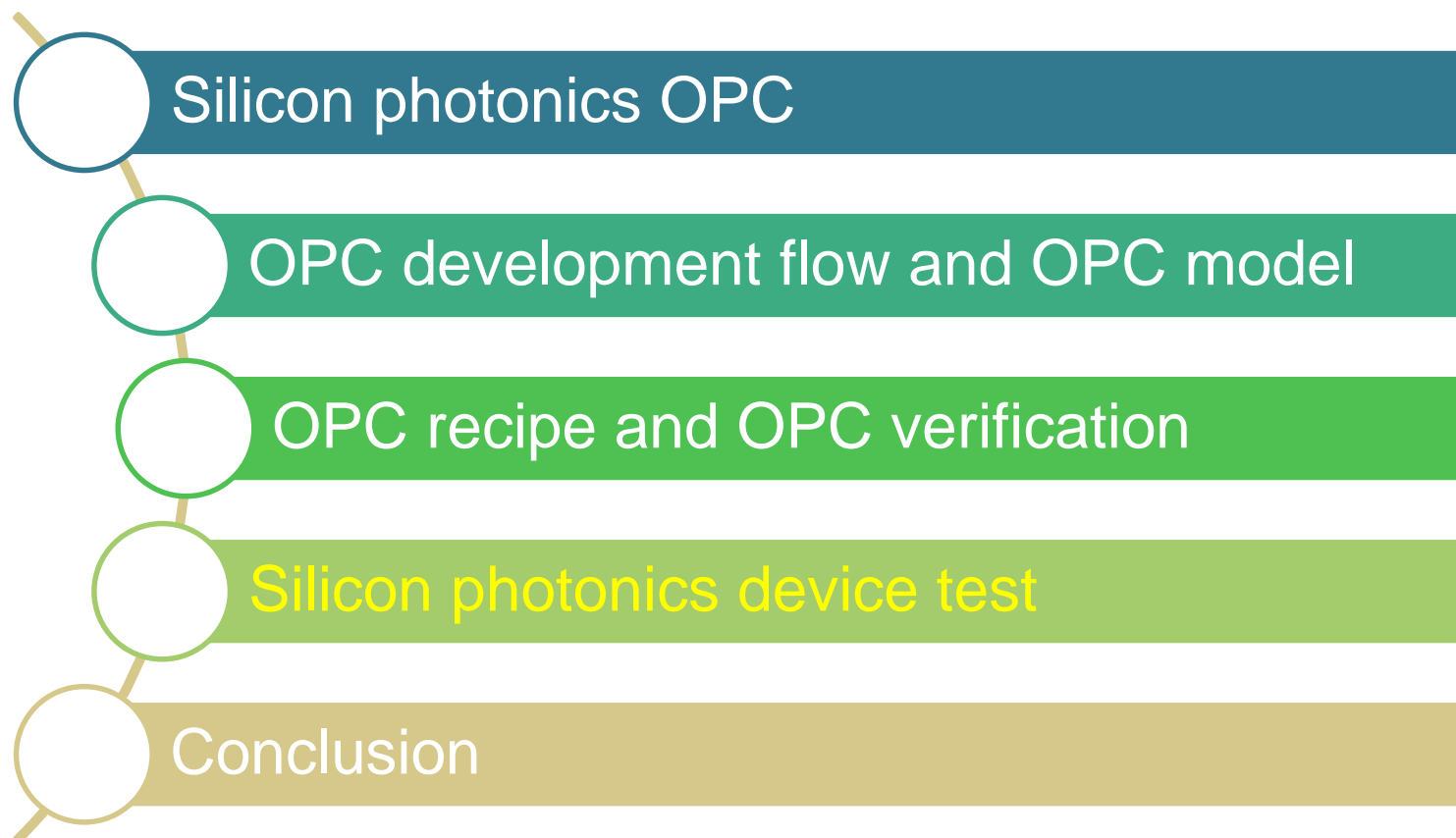


CD deviation

structure	type	drawing CD (nm)	noOPC AEI (nm)	Post OPC AEI (nm)
450nm waveguide	line	450	472.59	472.98
380nm waveguide	line	380	396.09	402.74
waveguide crossing	line	380	398.07	403.27
edge coupler	Line end	140	fail	163.9
180nm gap	space	180	169.56	166.04
200nm gap	space	200	201.69	188.22
directional coupler	space	190	186.43	180.13
AWG tip	space end	150	215.42	190.19
MMI tip	space end	150	205.19	166.22

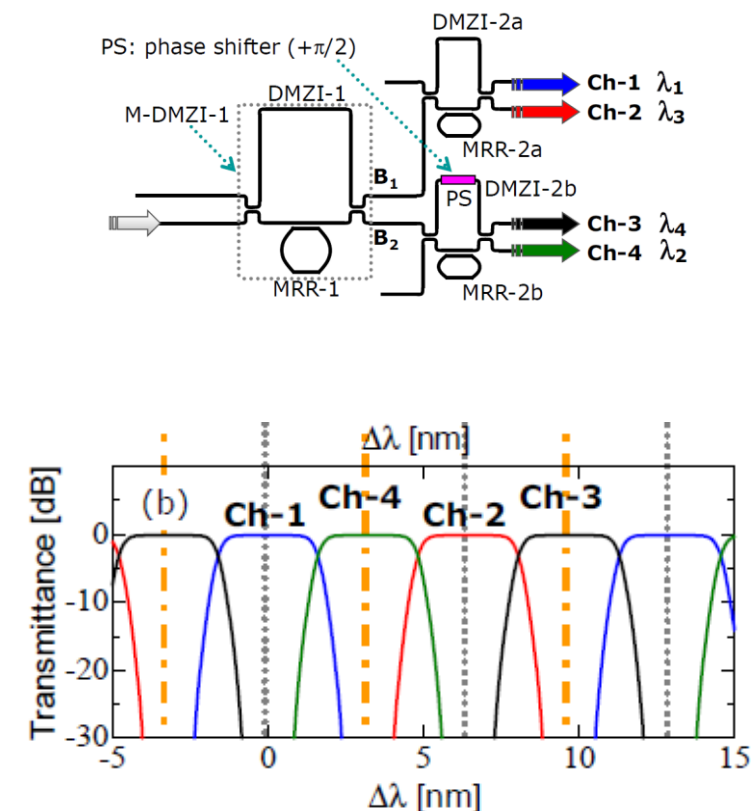
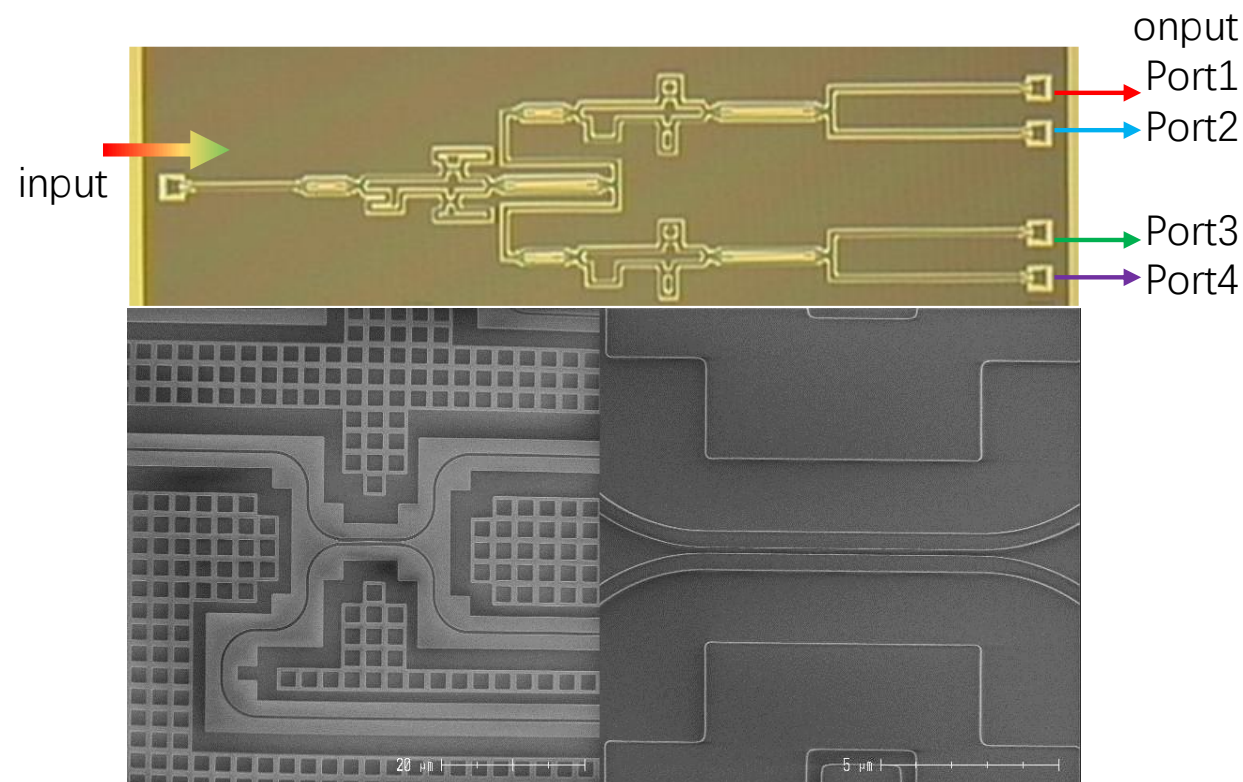
CD deviation (nm) = AEI CD - drawing CD





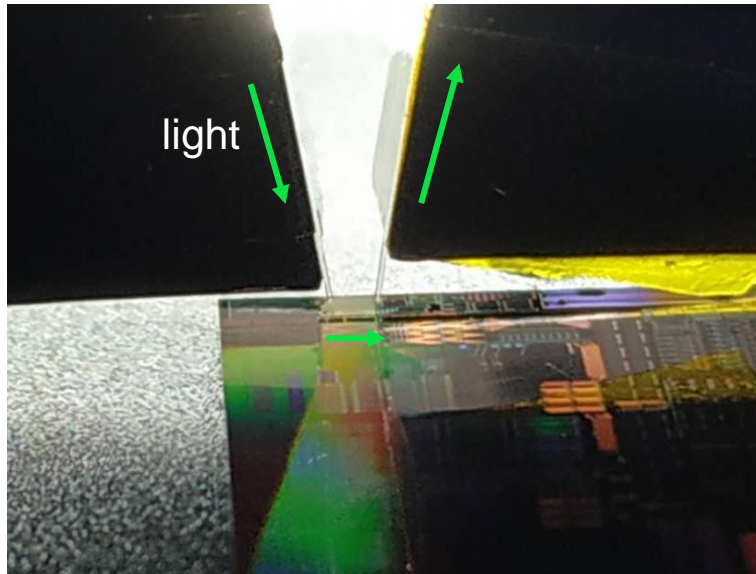
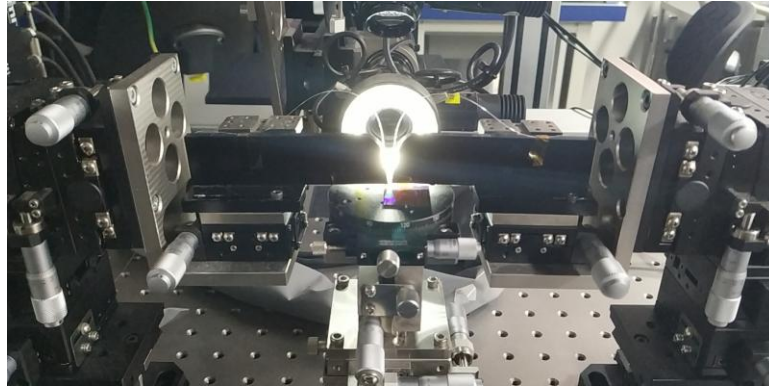
Optical test—CWDM device

- CWDM device-coarse wavelength demultiplexing device

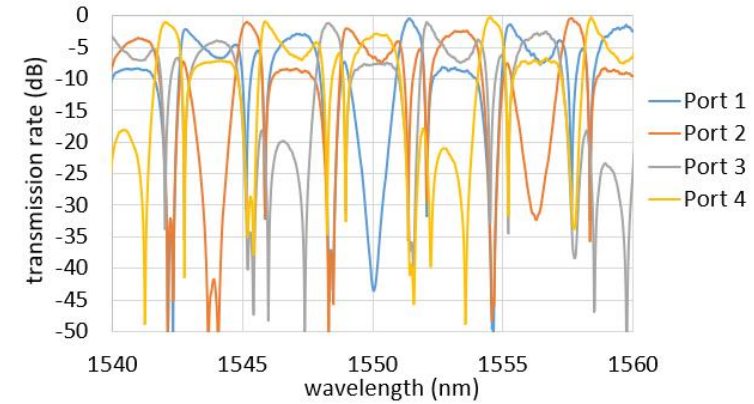


S. Jeong, S. Tanaka, T. Akiyama, S. Sekiguchi, Y. Tanaka, and K. Morito
“Flat-topped and low loss silicon-nanowire-type optical MUX/DeMUX
employing multi-stage microring resonator assisted delayed Mach-
Zehnder interferometers,” *Optics Express* Vol. 20, Issue 23, pp. 26000-
26011, 2012

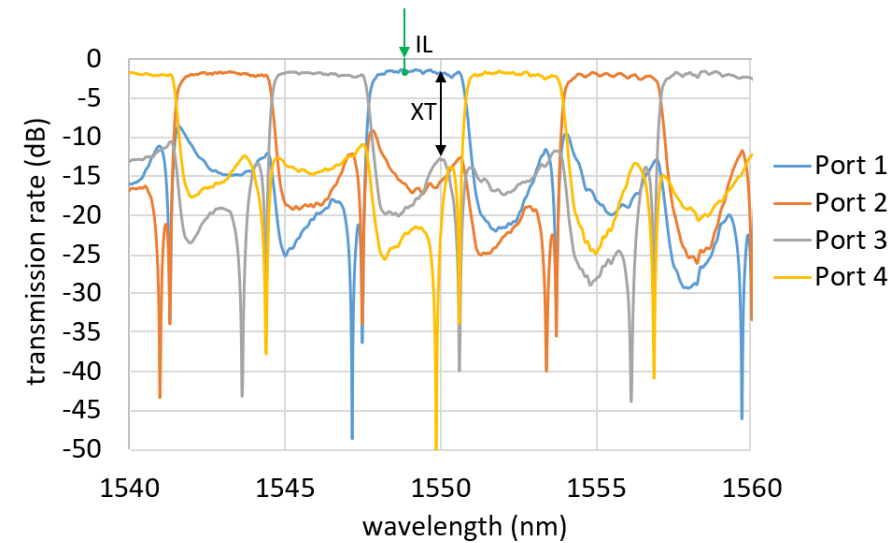
Optical test—CWDM device



no OPC



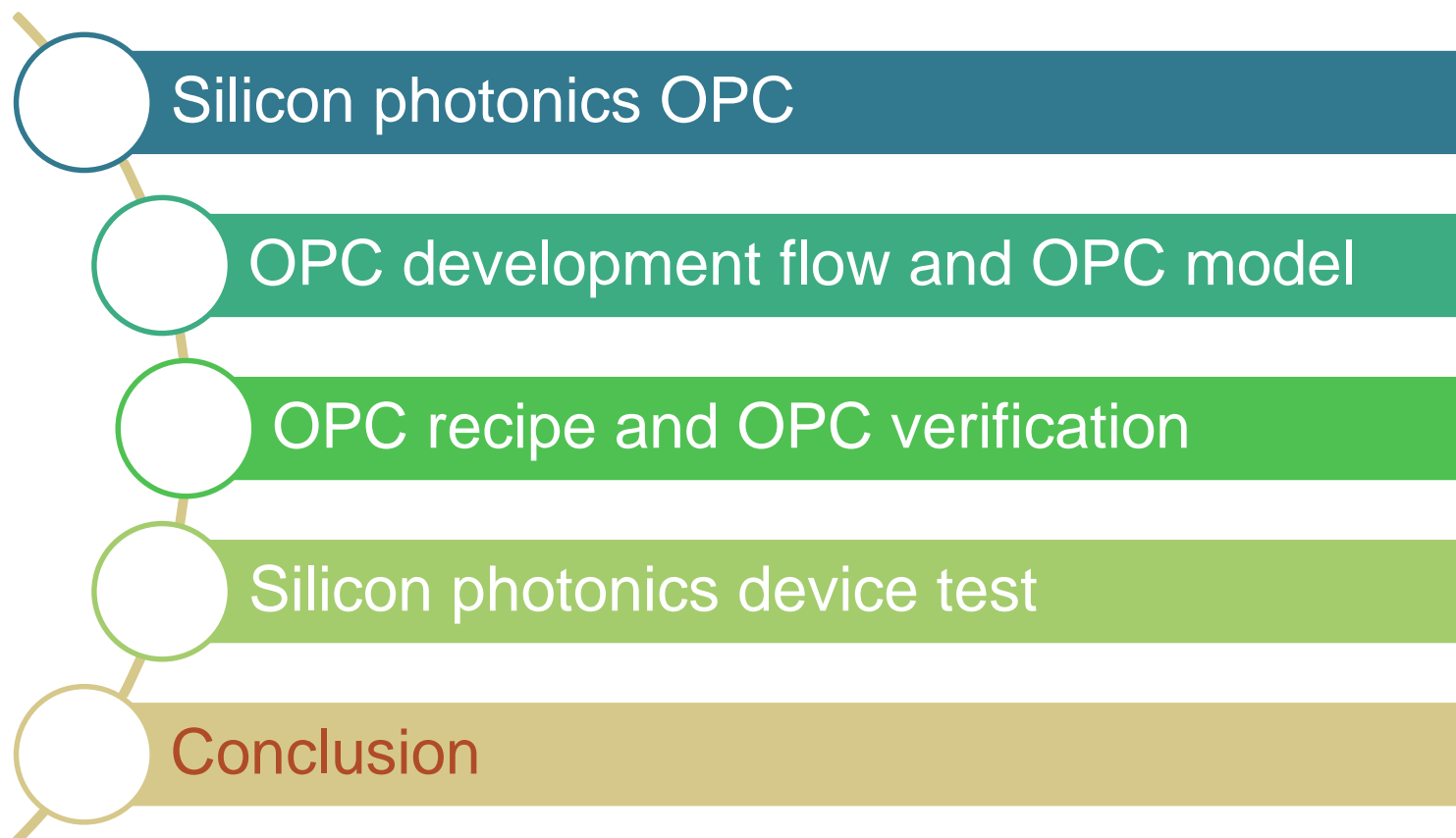
with OPC



crosstalk(XT) < -10 dB, insertion loss(IL) < 3 dB

Devices optical performances

devices	performance indexes	Performance evaluation	
		No OPC	OPC
waveguide(TE mode)	Transmission loss	baseline	comparable
1D/2D grating coupler	loss (efficiency of grating coupler)	baseline	improved
waveguide crossing	loss	baseline	improved
polarization beam splitter	Extinction ratio	baseline	improved
arrayed waveguide grating	Insertion loss, crosstalk	baseline	improved
CWDM	Insertion loss, crosstalk	baseline	improved



- We have generated a set of OPC model and recipe for the general silicon photonics devices. Two masks are used for preliminary OPC development-OPC test mask and OPC evaluation mask. Pixel based OPC method is suitable for silicon photonics devices because it can provide smooth sidewall configuration.
- OPC is beneficial for silicon photonics MPW platform and help promote devices performances.

	No OPC	180nm node OPC
CD accuracy	baseline	improved
Ultra-small feature fabrication	baseline	improved
fidelity of curvilinear structure	baseline	improved

- In CUMEC 180nm node silicon photonics MPW platform, with OPC, isolated line of about 140 nm can be fabricated.
- To further improve the device performance, 90nm and 130nm node silicon photonics OPC technologies are under development in CUMEC.

CUMEC Si photonics MPW

Tech.	2020							2021											
	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Active	30			29		24				10			16			14			14
Passive				29			15				6			7			19		





THANK YOU

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