Lithography and metrology for future process nodes

Mark Phillips

First SIA roadmap, in 1992

Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm²)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm²)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm²)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

For 50 years, semiconductor tool requirements have been driven by Moore's law.

Industry roadmaps predicted straightforward geometric scaling…

Intel Lithography Roadmap, Circa 2002

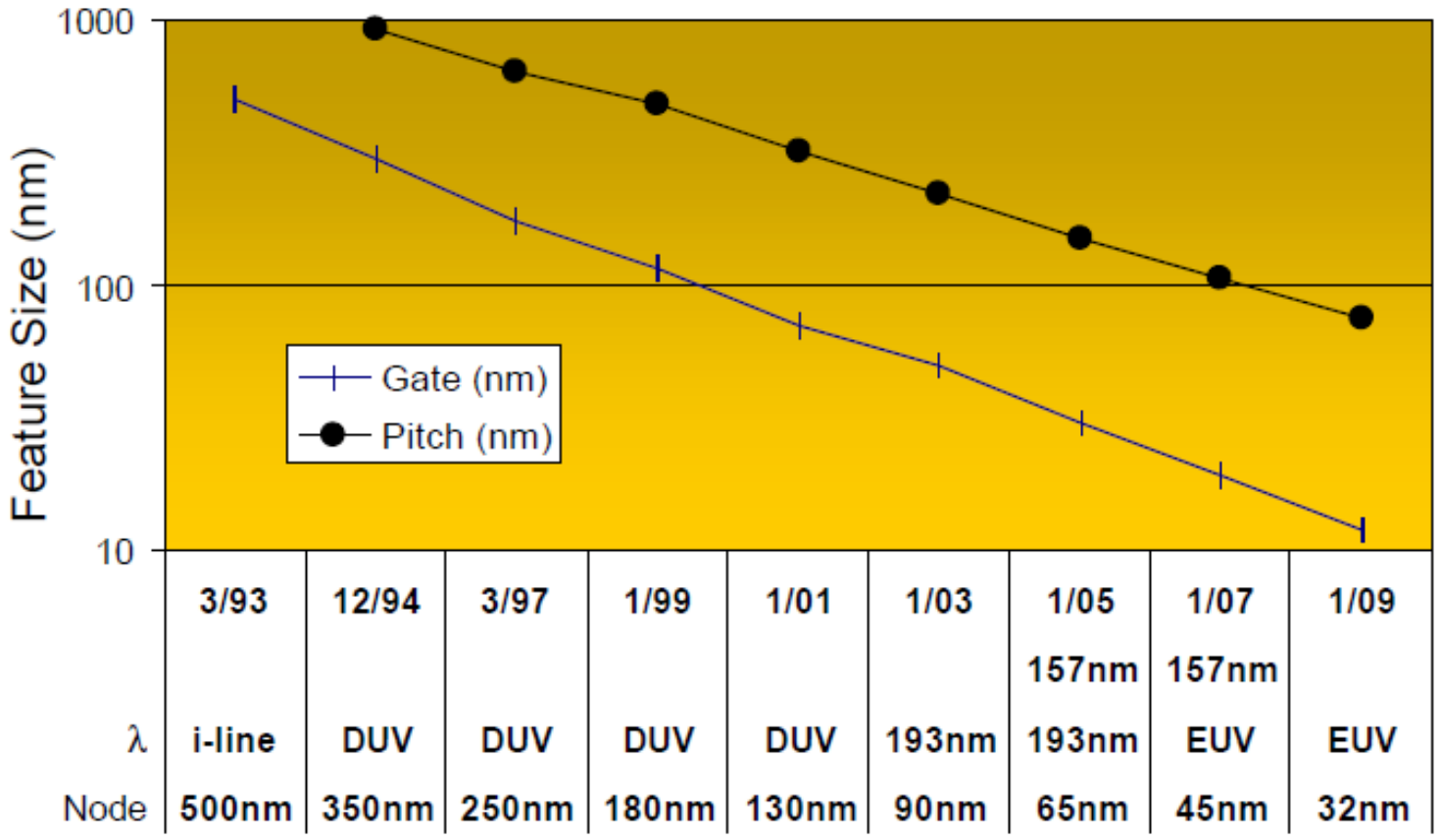


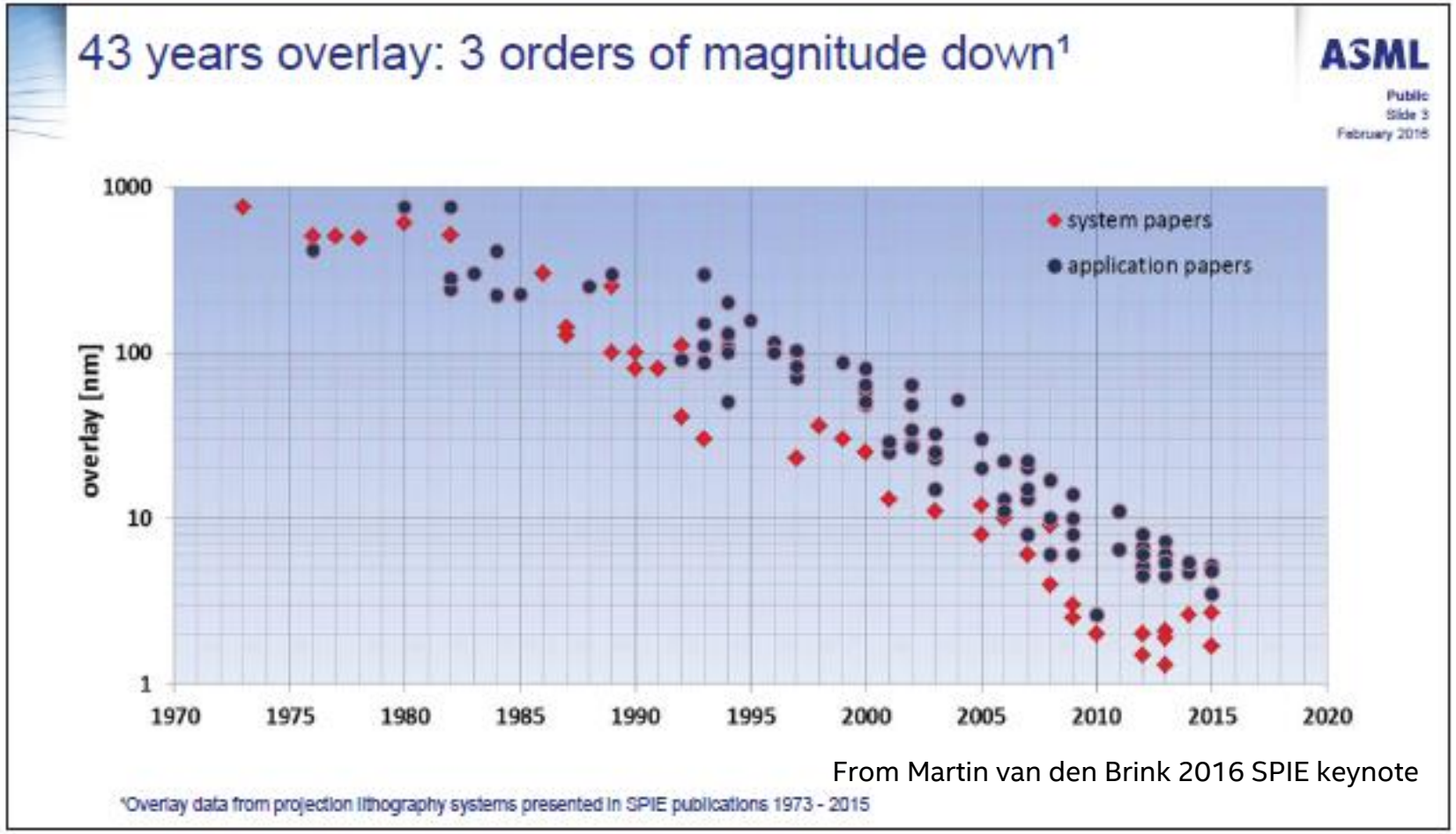
Figure 1: Intel Lithography Roadmap

Exposure tool roadmaps were derived from the device features and pitches in the industry roadmap using the Rayleigh criterion to determine λ/NA.

Though straightforward, they were not necessarily accurate predictions…

In practice, λ changed slowly, but lens NA increased dramatically with aspheres and immersion.

Exposure tool performance requirements



From Martin van den Brink 2016 SPIE keynote

- Other tool specs had to scale to enable use of resolution improvements
- Overlay, dose, and focus control are particularly important
- Most "On Product" performance improvements came from "system" improvements (i.e. those visible on a bare test wafer)

Metrology tool requirements

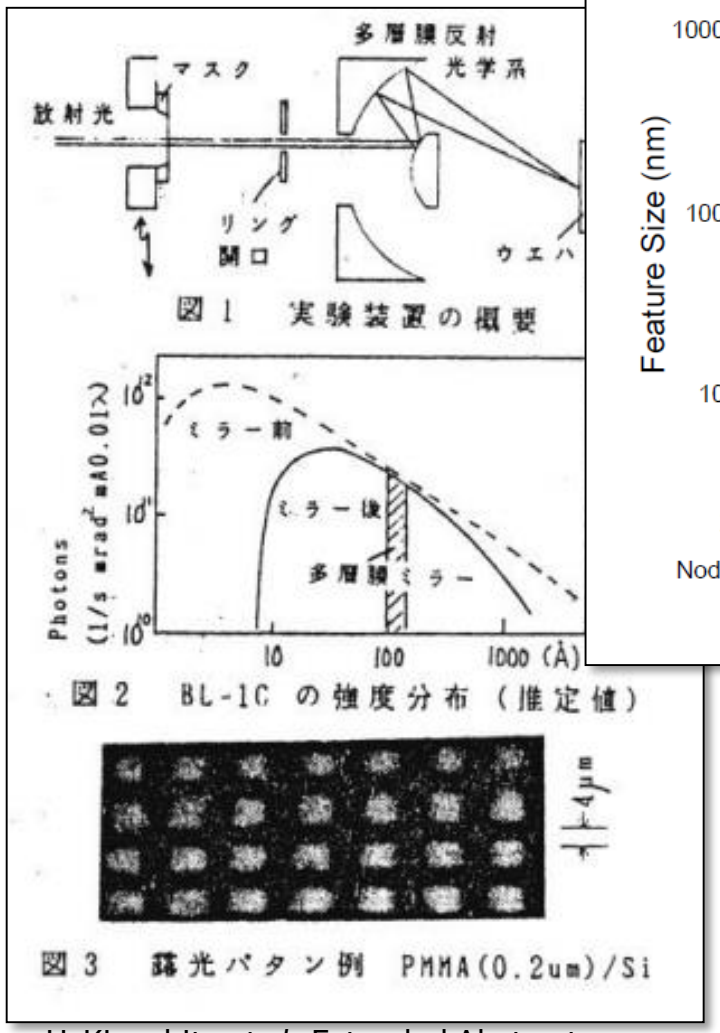
The Metrology Precision Roadblock

Year of First Product Shipment Technology Generation	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2003 100 nm	Driver
DRAM 1/2 Pitch	180	165	150	130	120	110	100	D½
Logic Isolated Lines	140	120	100	85	80	70	65	M Gate
Microscopy and Lithography								
Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	MPU
Front End Processes								
Logic Dielectric Thick Precision 1σ (nm) [B]	0.0025	0.0024	0.0021	0.0017	0.0016	0.0013	0.0012	MPU Gate
2D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	MPU Gate
Interconnect								
Barrier layer Thick (nm) process range (± 3σ) Precision 1σ (nm)	23 20% 0.08	19 20% 0.06	16 20% 0.05	13 20% 0.04	11 20% 0.035	7 20% 0.02	3 20% 0.01	MPU

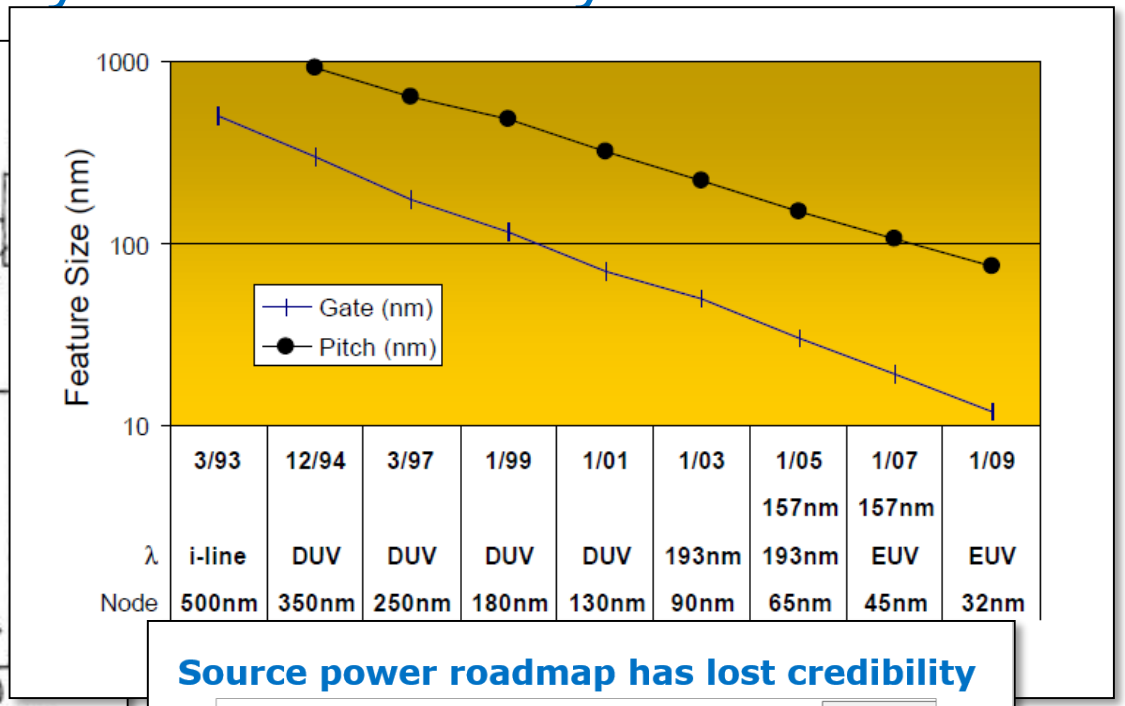
"Impact of the ITRS Metrology Roadmap", Alain Diebold, 2009 International Semiconductor Device Research Symposium

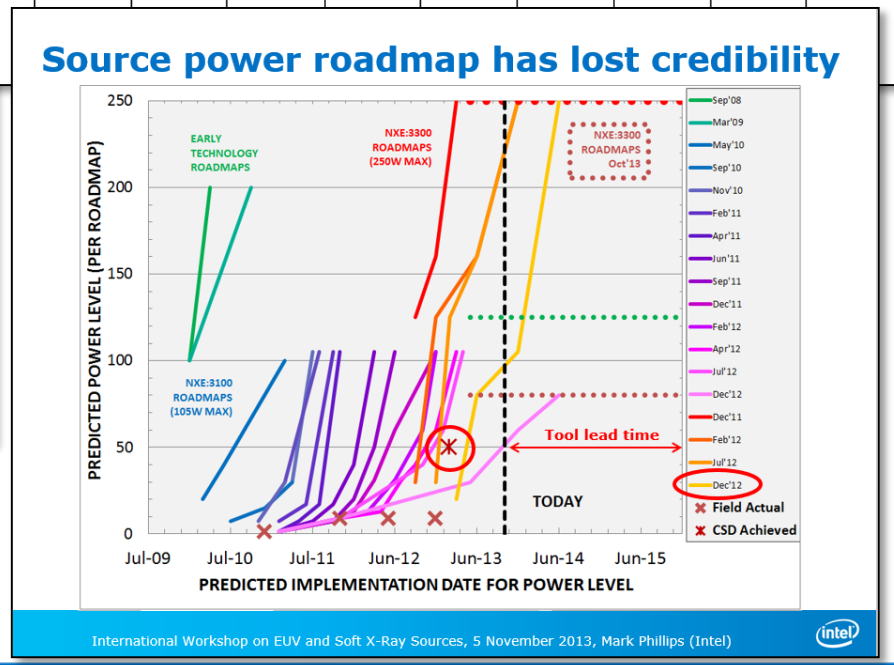
- Metrology tool requirements followed from required device feature control
- Set to consume no more than a fraction (e.g. 10 or 20%) of control budget
- Typically specs were on **precision** and **matching**, not **accuracy**, assuming optimal target would be determined by device performance/yield

Disrupted by EUVL delays



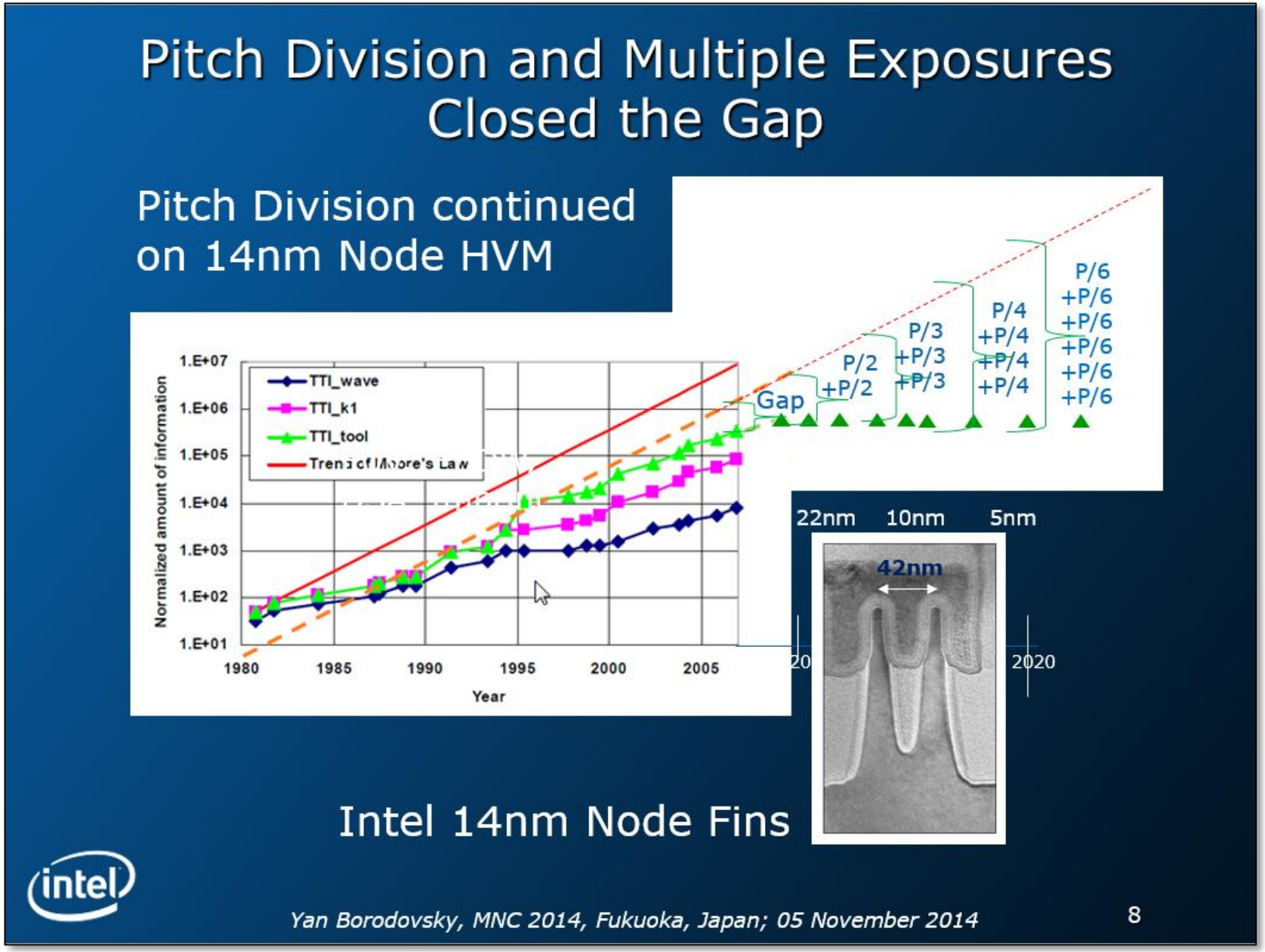
H. Kinoshita *et al.*, Extended Abstracts
The Japan Society of Applied Physics (1986)





- This (relatively) straightforward way-of-working was disrupted by long delays in EUVL
- When λ/NA stopped at 193nm/1.35, industry developed multi-patterning

Tool requirements for multi-patterning



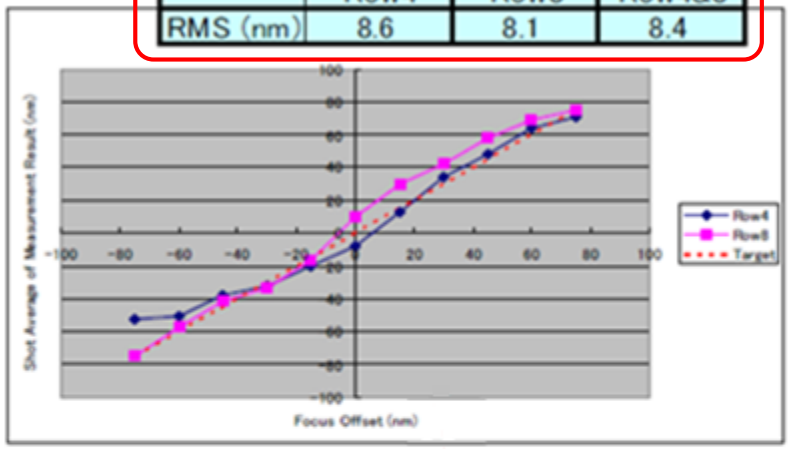
- Multi-patterning disconnects minimum device features from optical resolution, but it is **not free**.
- Feature **control** still needed to scale, forcing continued tool improvements
- Now on our 6th generation of 193i tool!

193i tool improvements

On-Product Focus performance for two generations of scanner

22nm node scanner

	Row4	Row8	Row4&8
RMS (nm)	8.6	8.1	8.4

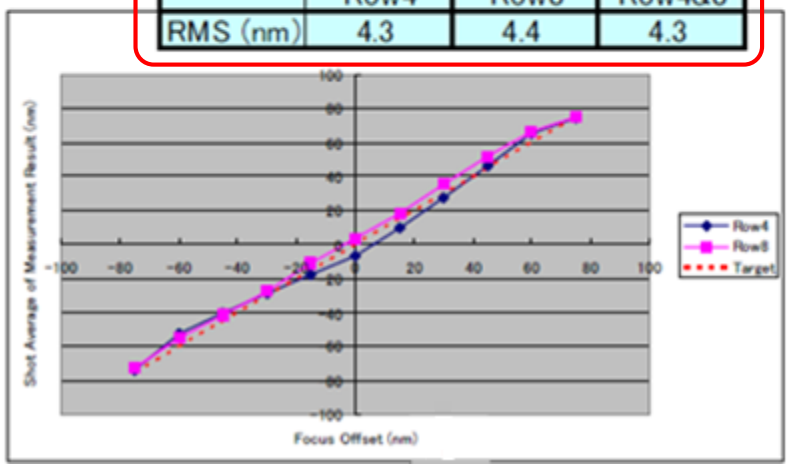


	Average (nm)	3Sigma (nm)
All shots	−1	42
Perfect shots	−2	39
Edge shots	4	46

By results in R ≤147mm

14nm node scanner

	Row4	Row8	Row4&8
RMS (nm)	4.3	4.4	4.3

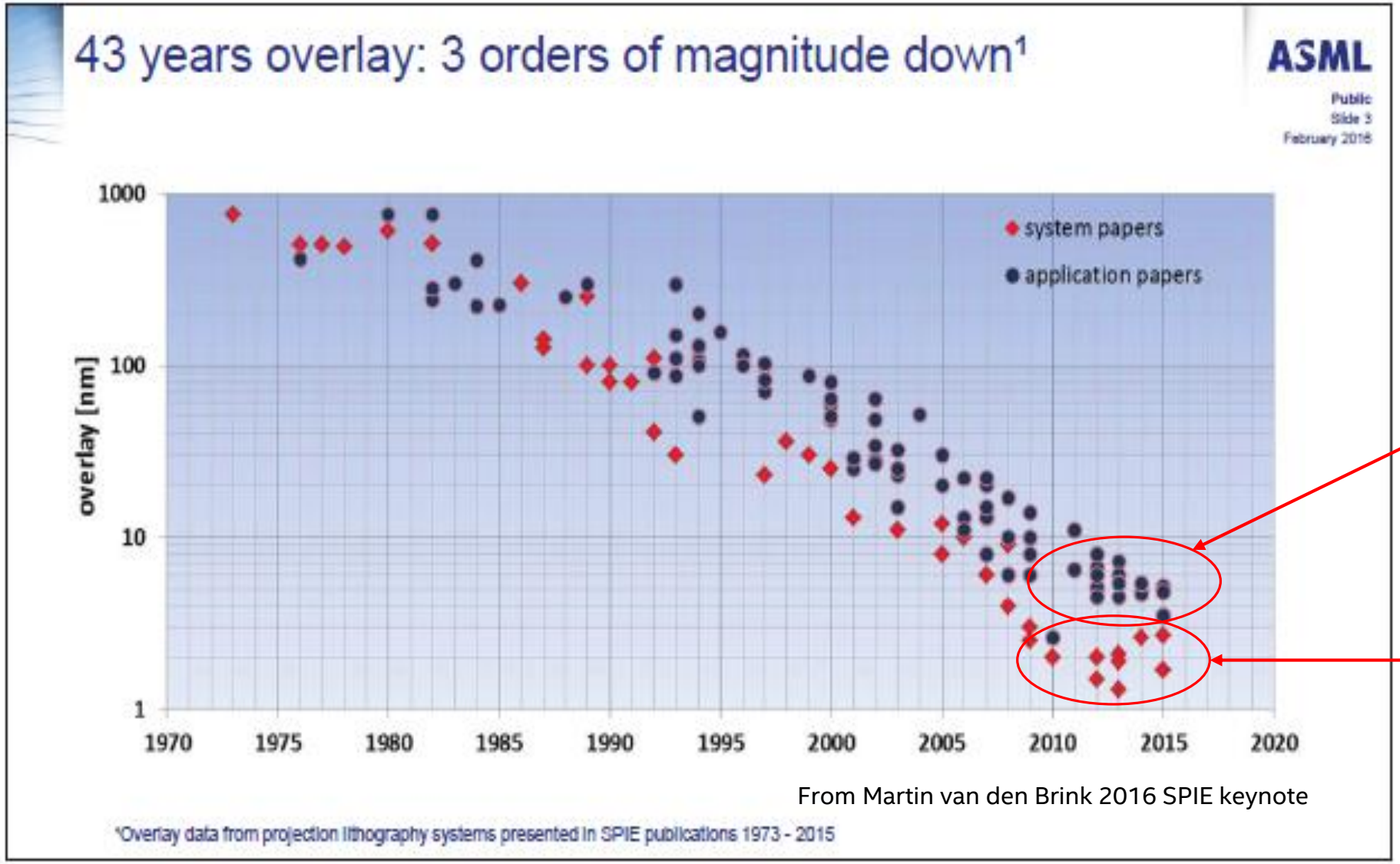


	Average (nm)	3Sigma (nm)
All shots	−6	25
Perfect shots	−7	23
Edge shots	−2	28

By results in R ≤147mm

- Use of 193i for multiple generations has required major tool improvements: especially overlay, focus, and productivity
- Further "system" improvements (visible on ideal test wafers) are now small and exponentially expensive
- Largest improvements now relate to on-product performance (focus example at left)

Shift to focus on “On-Product” performance



From Martin van den Brink 2016 SPIE keynote

Still a few nanometers of improvement possible in On-Product Overlay (OPO)

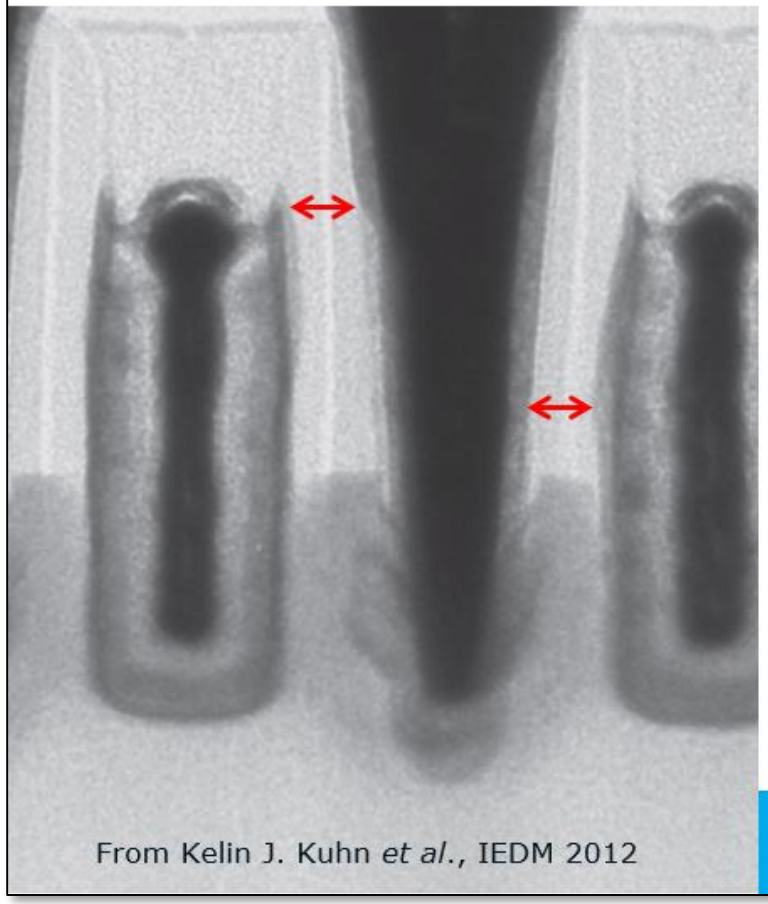
Little room left in “system” overlay

On-Product Performance

- Use of lithography exposure and metrology tools in production typically results in worse performance than seen on test wafers
- Many reasons for degraded performance: use of multiple production reticles, varying doses between previous and current layer, use of pellicles, and most importantly: **product wafers**
- Compared to bare Si test wafers, product wafers have degraded flatness, bow from stress, varying materials on back side (i.e. chucking surface), and a complex layer stack
- Improving tool performance on product wafers requires close collaboration between customer (who has product wafers) and supplier (who has System Engineers—this is not just an “Applications” problem)
- Scanner alignment and focus sensors are built-in metrology sensors, so there is synergy with current work on metrology accuracy in the presence of process variation (more on this later)

3D Device Edge Placement Error (EPE)

Edge Placement Error and Scaling



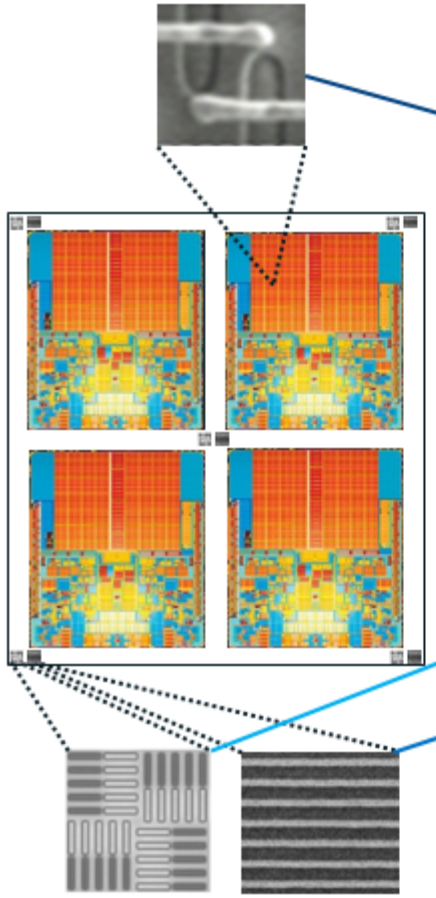
- Scaling is limited by accuracy of edge placement within device
- Things that should touch, must
- Things that shouldn't touch, can't
- This is a 3D problem, after litho, etch, TF dep, CMP, etc

Presented at 2013 ASML Technology Symposium

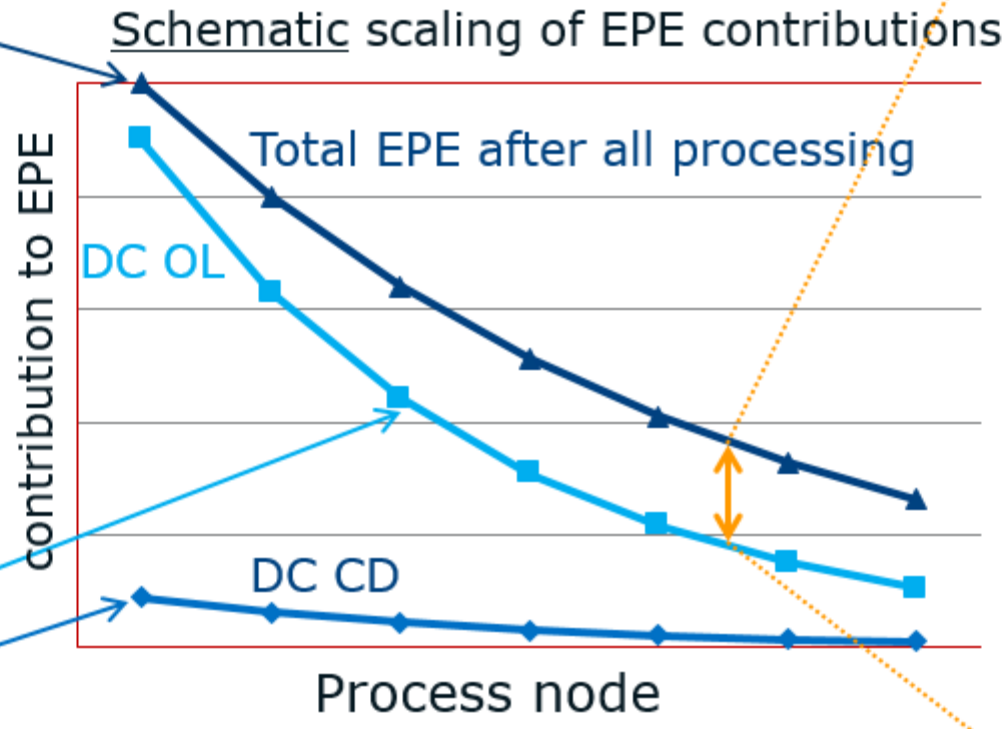
- Concept of 2D within-layer EPE in OPC had been around for many years
- In 2013, extended concept to 3D device structures (creating subsequent confusion)
- Goal was to explain overlay-*correlated* yield fallout even with in-spec overlay

Total Edge Placement Error vs DC CD & OL

Final device structure



scribeline targets



What is this "EPE gap"?

- Reticle error
- OPC modeling error
- OPE variation (X-field, T2T, tool stability)
- Scribeline target to device structure PW difference
- Etch (feature bias, x-wafer, chamber-to-chamber, stability)
- 3D: profiles, TF
- Shrink or freeze variation

Multiple patterning adds errors, with budgets specific to method: LELE, LFLE, SADP

As basic CD and OL performance of scanner has improved, relative magnitude of other contributions to EPE have grown

Presented at 2013 ASML Technology Symposium

Minimum pitch before and after multiple-patterning

- Prior to multi-patterning, minimum pitch in semiconductor devices was limited by lithographic resolution:

$$hp = \text{minimum pitch} / 2 = k_1 * \lambda / NA$$

- With multiple-patterning techniques, resolution is now limited by EPE and a process-dependent variable (p_1)

$$\text{minimum pitch} = p_1 * EPE$$

Based on presentation by Rich Schenker at 2016 Lithography Workshop

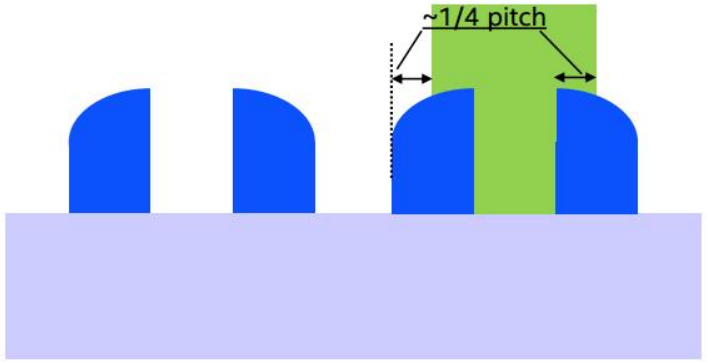
Pitch limitation with multi-patterning

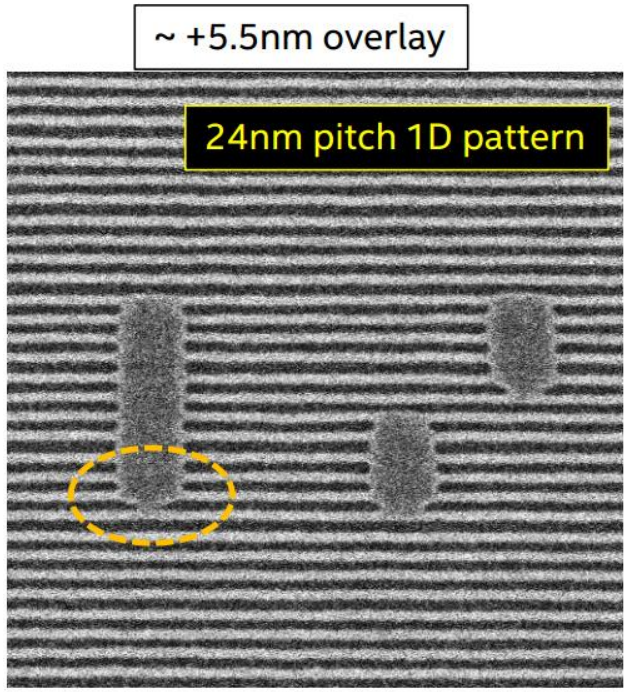
Min pitch vs EPE example

$$\text{Min Pitch} = p_1 * \text{EPE}$$

p_1 = process dependent variable
p_1 = ~4 for this process

Plug for Equal Line/Space





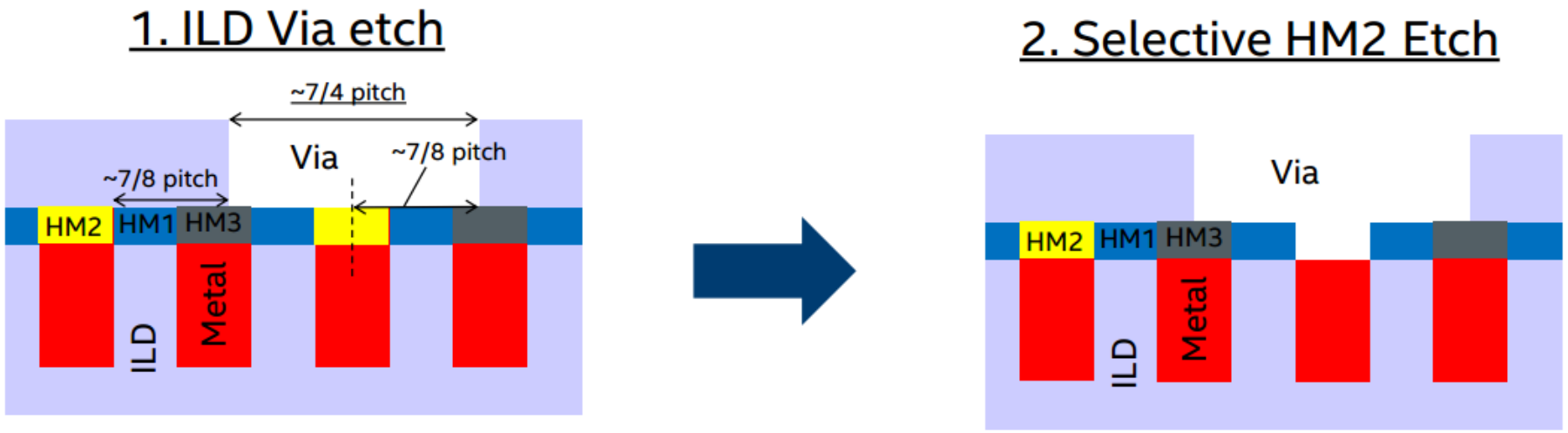
Schenker Litho Workshop 2016 26

- Instead of a simple equation based on optics, minimum pitch is now determined by the patterning scheme and EPE
- EPE is determined by the performance of all the tools in a particular patterning flow

Self-alignment and coloring reduce p_1, but…

6nm pitch example (colored pattern)

- Via size = ~¾ pitch (4.5nm) → ~7/4 pitch (10.5nm)
- Max EPE ~3/8 pitch (2.25nm) → ~7/8 pitch (5.25nm)
- Requires multi-direction selective etches.
- Requires at least 2 Via litho exposures.



- add additional sources of EPE variation
- add materials challenges and process complexity

Suppliers need to address EPE on process wafers

Summary of EPE discussion

- The key challenge to continued dimensional scaling is EPE
- With multiple-patterning techniques, the minimum pitch useable in a device is p_1 * EPE
- The p1 factor depends on the process, and can be significantly increased with clever process techniques, but usually with some increase in complexity
- The exposure tool is a key contributor to EPE, as is process variability, and the interaction between the exposure tool, metrology, and process variability
- This creates an opportunity for ASML to add value to customers by expanding the scope of their products to address these tool/metrology/process interactions (hence Brion, YS, HMI, etc)

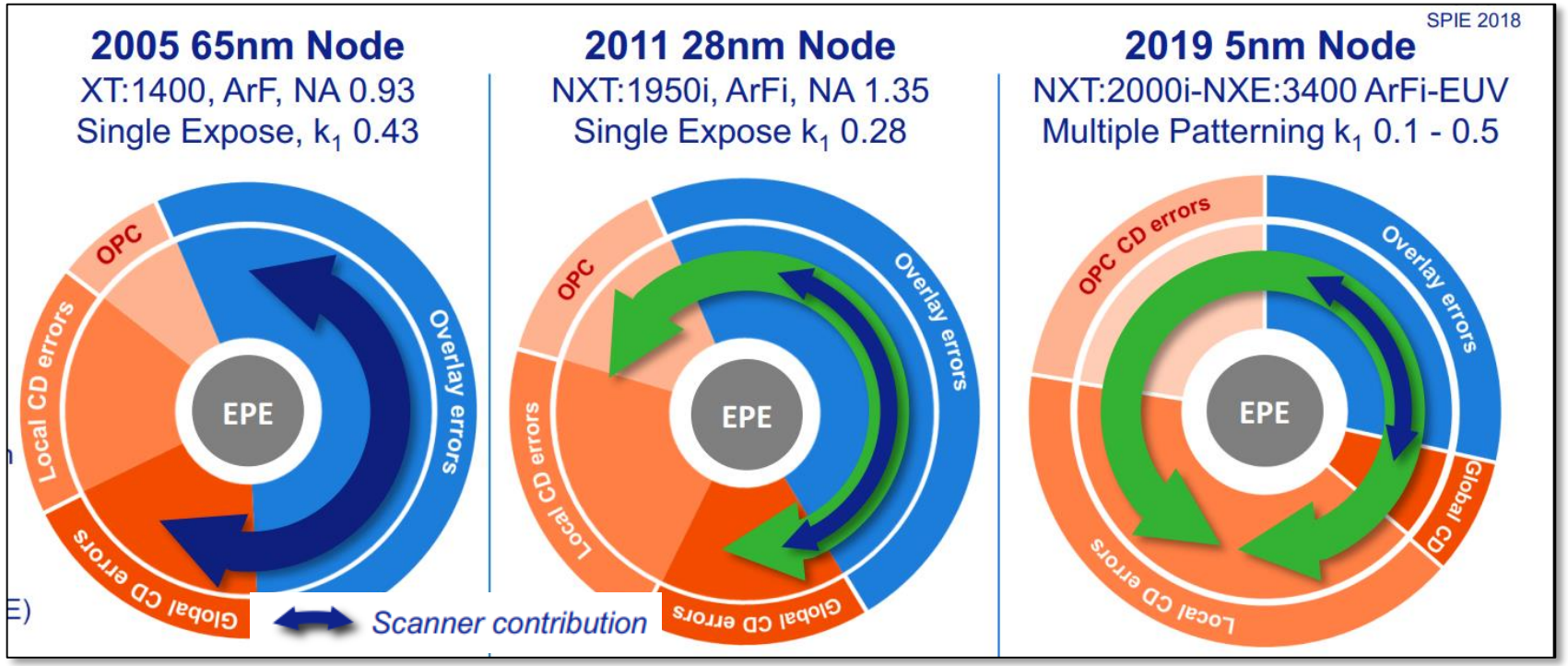
Example guidance to a supplier internal engineering conference

So what does a real EPE budget look like?

From Jan Mulkins, 10585-55, SPIE Advanced Litho 2018

- Highly proprietary, so unlikely to see a public disclosure based on a leading-edge production node
- Pie-chart at left is based on ASML study of the IMEC iN7 logic device (corresponds to 5nm “foundry” node)
- Stochastics is the largest contributor for this example (more on this later)
- How has this evolved over time?

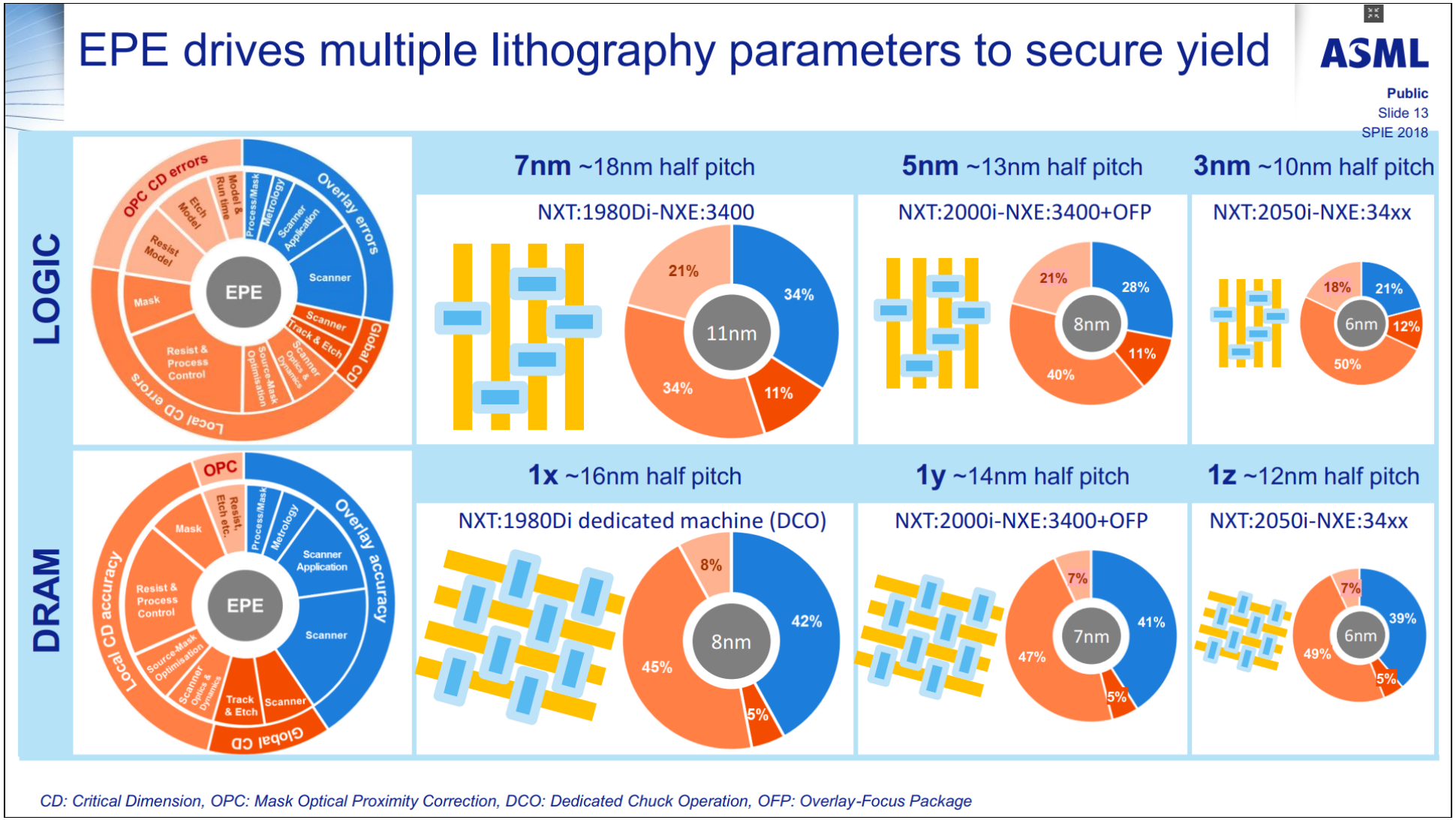
Looking backward at 3D device EPE…



From Martin van den Brink, 2018 SPIE Advanced Lithography

- >10 years ago, scanner (particularly overlay) dominated budget
- Many engineers still think of the problem this way, even though scanner contribution dropped below 50% even before multi-patterning
- Stochastics (Local CD) increasing rapidly, followed by OPC errors

EPE looking forward…

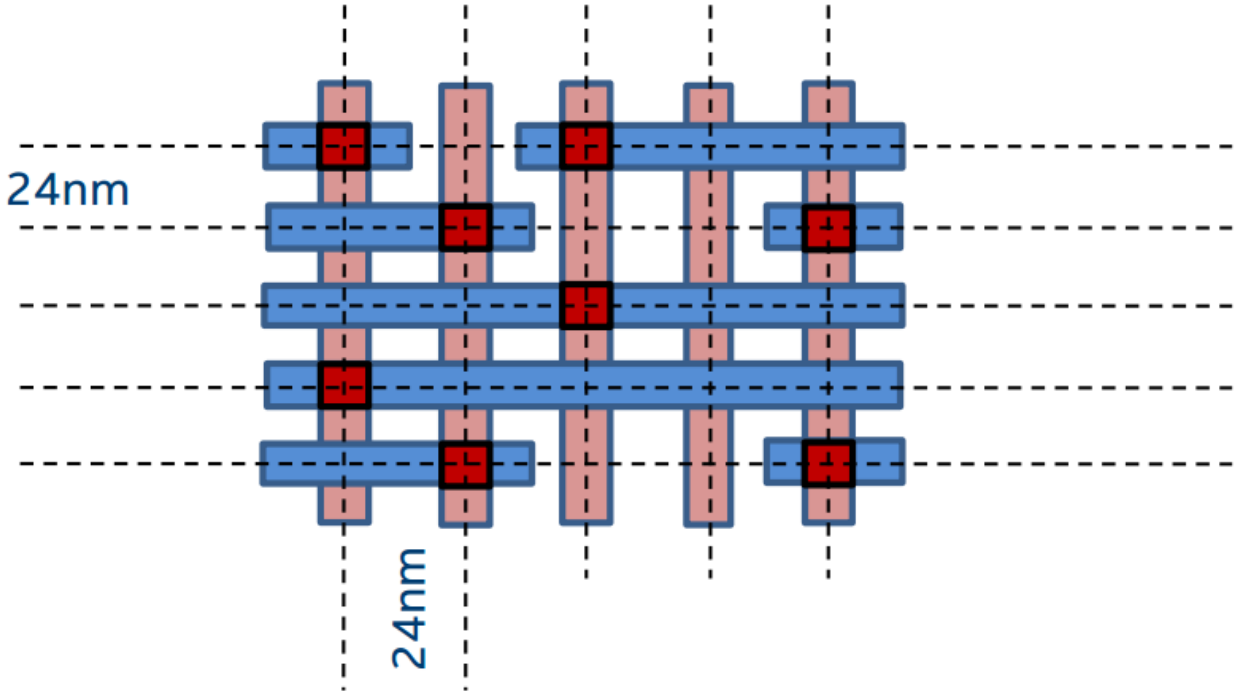


From Martin van den Brink, 2018 SPIE Advanced Lithography

- Details differ by device type and node
- Stochastics ~50% of budget for second EUV node

EPE must include stochastics with trillions….

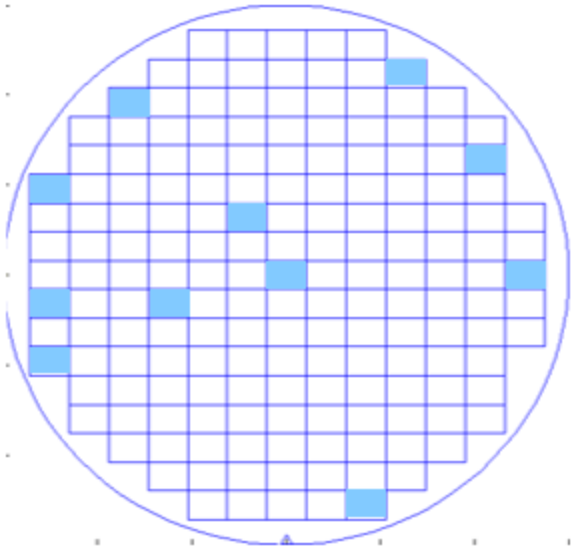
- With a 24x24nm metal pitch grid, there are 123 trillion possible overlap locations on a 300mm wafer.
- If 1 in 6 has a Cut or Via, there are 20 trillion Cuts or Vias on the wafer.
- ~40,000 occurrences of 20 trillion are outside +/- 6σ normal distribution.



Trillions of features need ppTrillion-type failure rates

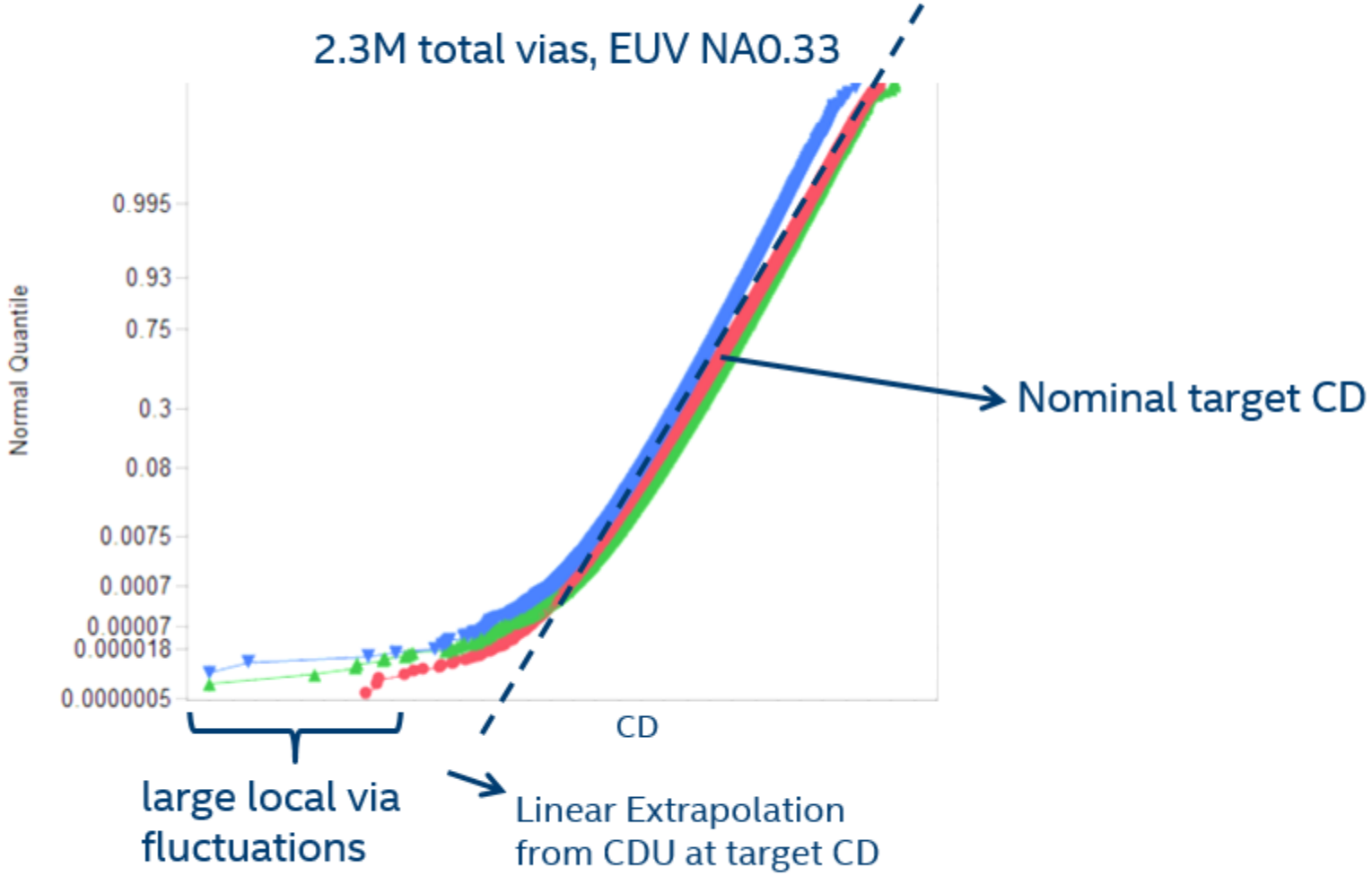
- Good process: Majority of die work at the end of many litho passes
- Therefore, can only tolerate of order ~1 via failure per litho pass (logic).

Case	λ nm	NA	p_{min}	Nvia (T)	via fail rate (ppTrillion)
193	193	0.93	104	0.07	15
193i	193	1.35	71.5	0.14	7
EUV_{now}	13.5	0.33	20.5	1.7	0.6
EUV_{later}	13.5	0.55	12.3	4.7	0.2



Generic yield map for illustrative purposes

2.3M actual vias: Effect seen in tail CD distribution.



Implications of 7 Sigma process requirement

- Tools must be designed to support a process requiring PPT-level EPE failures ("7 sigma", though the tail is likely not consistent with a normal distribution)
- This is not a request to replace 3σ with 7σ in every design budget.
- Request is for suppliers to comprehend the importance of the extreme tail of the EPE distribution to Intel's use case
  - Understand what drives this distribution at the ppT level
  - Create a budget for this distribution tail to identify and prioritize improvement opportunities
- This is especially important to take full advantage of 0.33NA EUV and to make High NA EUV successful

How can High-NA help?

High-NA EUV enables 2 nodes of shrink

for random cut mask applications

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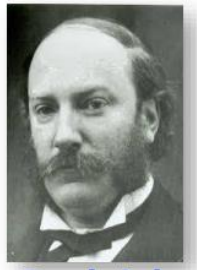
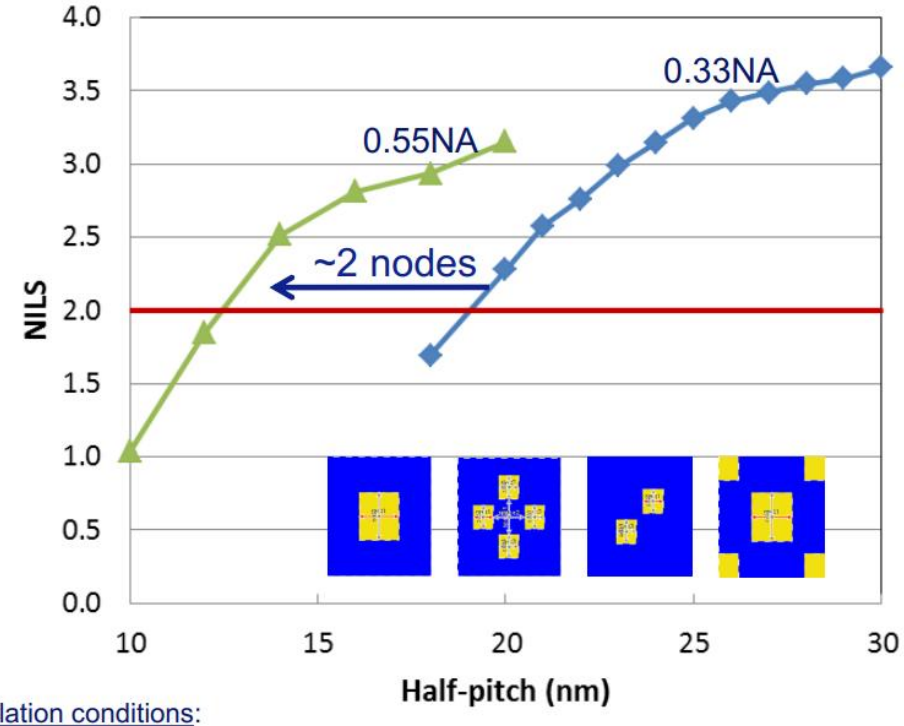
SPIE 2018



Rayleigh

$$CD = k_1 \frac{\lambda}{NA}$$

- Selection of cut mask features
- NA gain shown for minimum pitch



Simulation conditions:
- Conventional illumination
- No SMO applied

Jan van Schoot, 2018 SPIE Advanced Lithography

- EUV photon statistics increase stochastic effects, but improved resolution eliminates EPE hit from pattern splits
- This is true for 0.33NA EUV vs 193i, and will be true for 0.55NA vs 0.33NA

High-NA contrast & dose benefits to stochastics

Larger NA reduces Local CDU

Due to larger aerial image contrast

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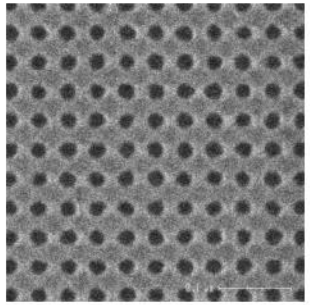
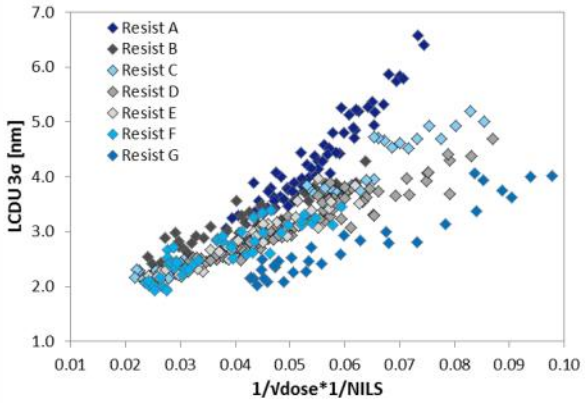
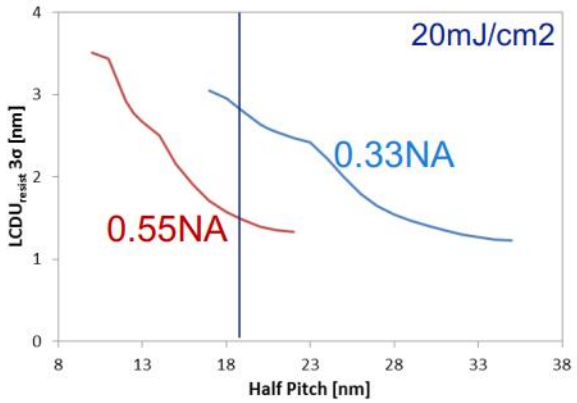
resist dose contrast

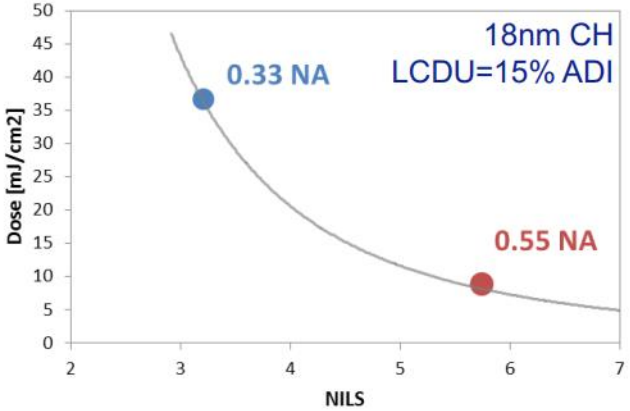
$$LCDU\ (nm) \approx \sqrt{\frac{h\nu}{\alpha}\left(1+\frac{1}{QE}\right)}\ \sqrt{\frac{1}{E_{size}}}\ \frac{1}{NILS}$$



Non-CAR resist, Quasar Illumination







Jan van Schoot, 2018 SPIE Advanced Lithography

- Improved contrast reduces LCDU for a given feature (at constant dose)
- Improved optics transmission and source progress should allow higher dose
- Need continued resist progress (ongoing on MET5 at Intel)

EPE challenge sparks "Golden Age" for metrology

Metrology requirements for EPE control

Metrology data is vital to managing the EPE budget

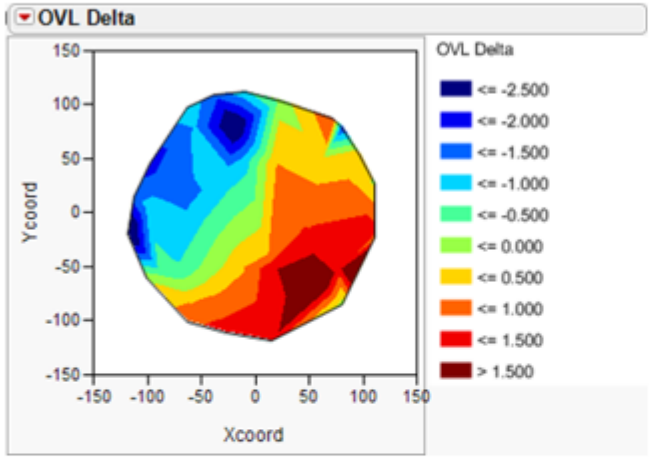
- Need more data (→ low MAM time and tool cost)
- Need smart sampling (quantify all systematic errors, but only measure at appropriate frequency)
- Need absolute accuracy in addition to precision and matching
  - EPE budgeting is not valid if there are unquantified biases, and resulting budget will not accurately predict yield
  - Process control based on biased metrology will not result in optimal yield
  - Variation in process/metrology interaction degrades process control

KLA-Tencor Lithography Users Forum Slide 11 22 February 2015, Mark Phillips

- For several decades, fabs regarded metrology as "non-value-added"—as little as possible, as cheaply as possible
- Metrologists had worried about accuracy for years, but fabs focused on precision (e.g. "TMU")
- When yield is limited by EPE, better metrology has a compelling ROI

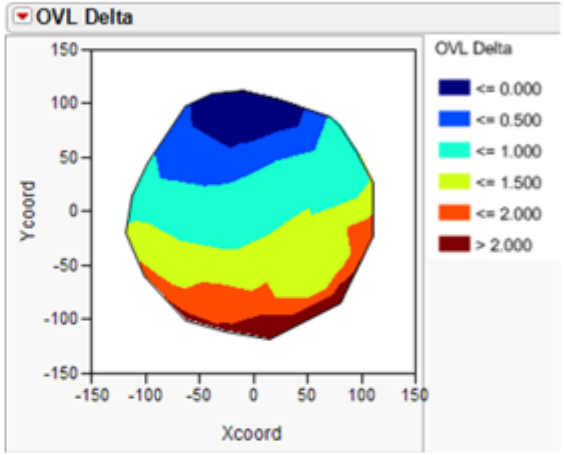
Example of accuracy vs TMU in overlay metrology

SbS Overlay Deltas between two low-TMU conditions



X OVL Deltas

Linear Term Deltas:
Xscale: 0.01ppm
WfrSkew: 0.012ppm
MaxError: 2.3nm



Y OVL Deltas

Linear Term Deltas:
Yshift: 0.9nm
Yscale: 0.01ppm
MaxError: 0.3nm

- SbS overlay deltas are systematic and fit a typical linear model
- **Differences in modelled errors are ~2nm, which is 5-10X TMU!**

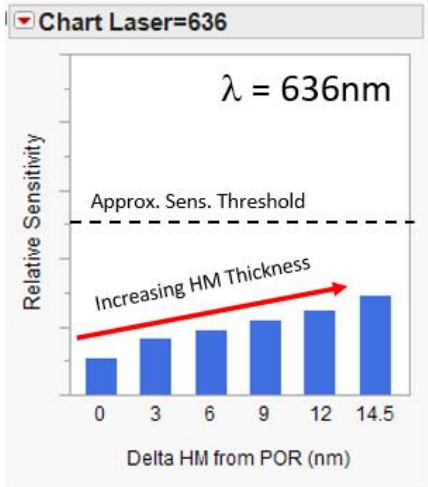
KLA-Tencor Lithography Users Forum Slide 17 22 February 2015, Mark Phillips

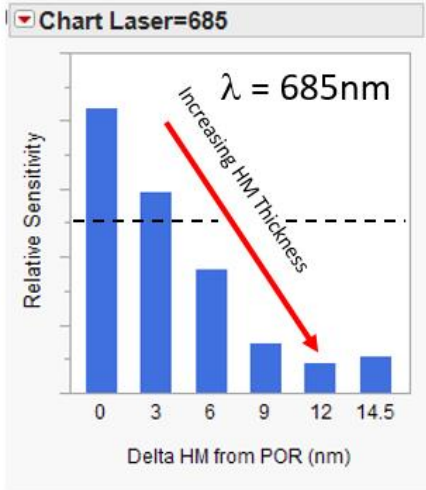
- Comparison of two very precise measurement conditions shows at least one (maybe both—who knows?) are wrong
- 2nm is a catastrophic mis-targeting on a modern process node
- Errors are caused by sensitivity of measurement physics to stack and feature variation (WTW and WIW)

Wavelength flexibility

Better Metrology: Process/Stack Sensitivities

- But with limited wavelengths, expect some recipes to be unrecoverable
- Not a physical limitation (e.g. absorption). Diffracted light exists but lacks sensitivity to overlay





OVL Sensitivity vs. Hardmask Skew by Wavelength: **Layer 2**

For this layer, available wavelengths do not recover sensitivity
Need maximum flexibility in wavelength selection

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LithoVision | 2016

- Asked for flexible wavelength hoping to find optimal measurement conditions
- Flexibility is helpful, but found that in many cases, no single wavelength produces accuracy robust to process variation
- However, studying accuracy through wavelength yielded an important result…

Multi-wavelength measurements provide robust accuracy

Multi Wavelength approach towards accuracy & robustness

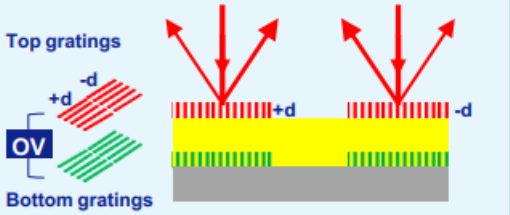
ASML

Public
Slide 6

Enabled by continuous WL and fast WL switching hardware (reducing throughput penalty)

DBO uses overlapping gratings with a shift(bias) +*d* and -*d*

$A^+ = K(OV+d)$ $A^- = K(OV-d)$



- *K is overlay sensitivity: detects process dependency of overlay*
- *A is asymmetry (delta intensity)*

$$OV = d \times \frac{A^+ + A^-}{A^+ - A^-}$$

Slope is proportional to overlay in A^+ vs. A^- plot

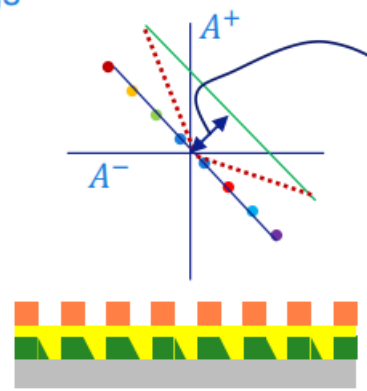
Slope of the line => Overlay

Symmetric gratings

$$A^+ = \left(\frac{OV+d}{OV-d}\right) A^-$$

Each colored dot is a different WL

Every WL has the same slope to origin = same OV



Asymmetric gratings

$$A^+ = \left(\frac{OV+d}{OV-d}\right) A^- + C$$

Every WL has different slope to origin = wrong OV

Distance to origin (DTO) = measure of asymmetry ~ C

Multi WL (at least dual WL) can describe the OV more accurately than 1 WL

Slope of multi WL line immune to asymmetry= accurate OV

Note: On very limited cases, where high asymmetry is present, a non-linearity in behavior above is observed; it is covered under advanced activity and kept out of scope for this paper

SPIE Advanced Lithography, 2018

From Kaustuve Bhattacharyya, 2018 SPIE AL

- Combining information from different wavelengths provides robust accuracy
- Site-by-site run-time metrics indicate when excessive process variation breaks assumptions

Scanner alignment sensors are metrology tools too…

Metrology/Process interaction is limiting On-Product Overlay

- State-of-the-art On-Product Overlay (OPO) performance is several nanometers higher than MMO on test wafers
- OPO-to-MMO gap is dominated by W2W and L2L variations much larger than scanner stability
- Process variation interacts with metrology--both alignment sensors on scanners and resist overlay metrology tools—and is convoluted in OPO
- Site-by-site accuracy metrics should be applied to scanner alignment in addition to overlay measurement

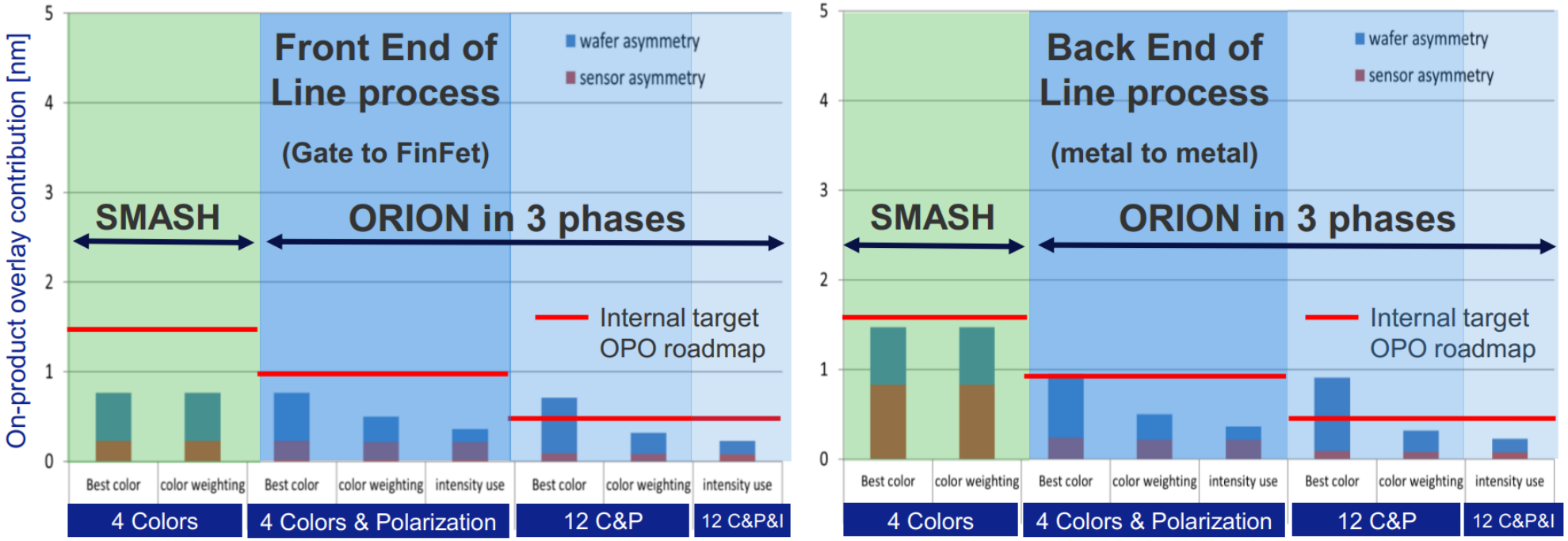
KLA-Tencor Lithography Users Forum Slide 29 22 February 2015, Mark Phillips

...so ASML is adding colors & polarizations,

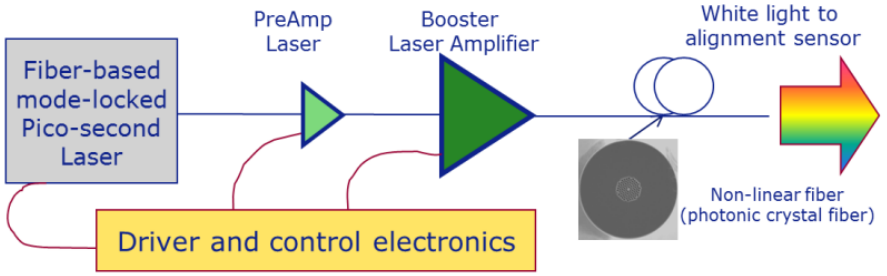
Alignment system improvement roadmap in 4 steps

ASML

Public
Slide 30
SPIE 2018



We will move from 4 solid-state lasers to an multi-color white light source to extract up to 12 colors



...while Nikon adds inline & standalone metrology

New Functions and Benefits

Overlay improvement

Alignment mark asymmetry detection
- Scatterometry optics
- Metrology error correction

Topography measurement

High resolution topography measurement
- Extremely high spatial resolution
- Device feature, edge profile can be measured

Film thickness monitoring

Spectral reflectance metrology
- P/S polarized spectrometry optics
- Film thickness can be calculated

Nikon 17 LithoVision | 2018

Nikon ArFi Scanner : NSR S635E

Pre mea
- Dense s
- High or

EGA on t
- Sparse
- Linear c

Improved S631E
- ✓ Overlay
- ✓ Throughput
- ✓ Focus and imaging control ...

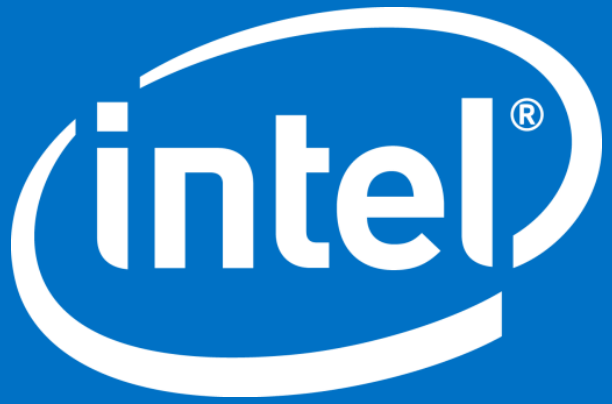
S635E was born targeting the next generation OPO budget

Nikon 5 LithoVision | 2018

From Yuichi Shibazaki, 2018 LithoVision

Summary

- For several decades, litho exposure tool requirements were based on λ/NA reduction–on timing guided by Moore's Law scaling–with other tool and metrology requirements set to support the target resolution.
- This straightforward way of working was first disrupted by multi-patterning, which was developed to continue scaling while waiting for EUVL.
- As tool overlay performance dipped into single-digit nanometers, other sources of error became a significant part of the 3D device EPE budget.
- For future process nodes, exposure and metrology tool requirements are based on the need to deliver 7σ EPE consistent with the node design rules.
- To support accurate EPE budgeting and control, metrology tools need to maintain accuracy in the presence of process variation
- Recent metrology learning on accuracy and process-robustness needs to be extended to exposure tool on-board metrology (alignment and focus)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